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EDN

VOICE OF THE ENGINEER

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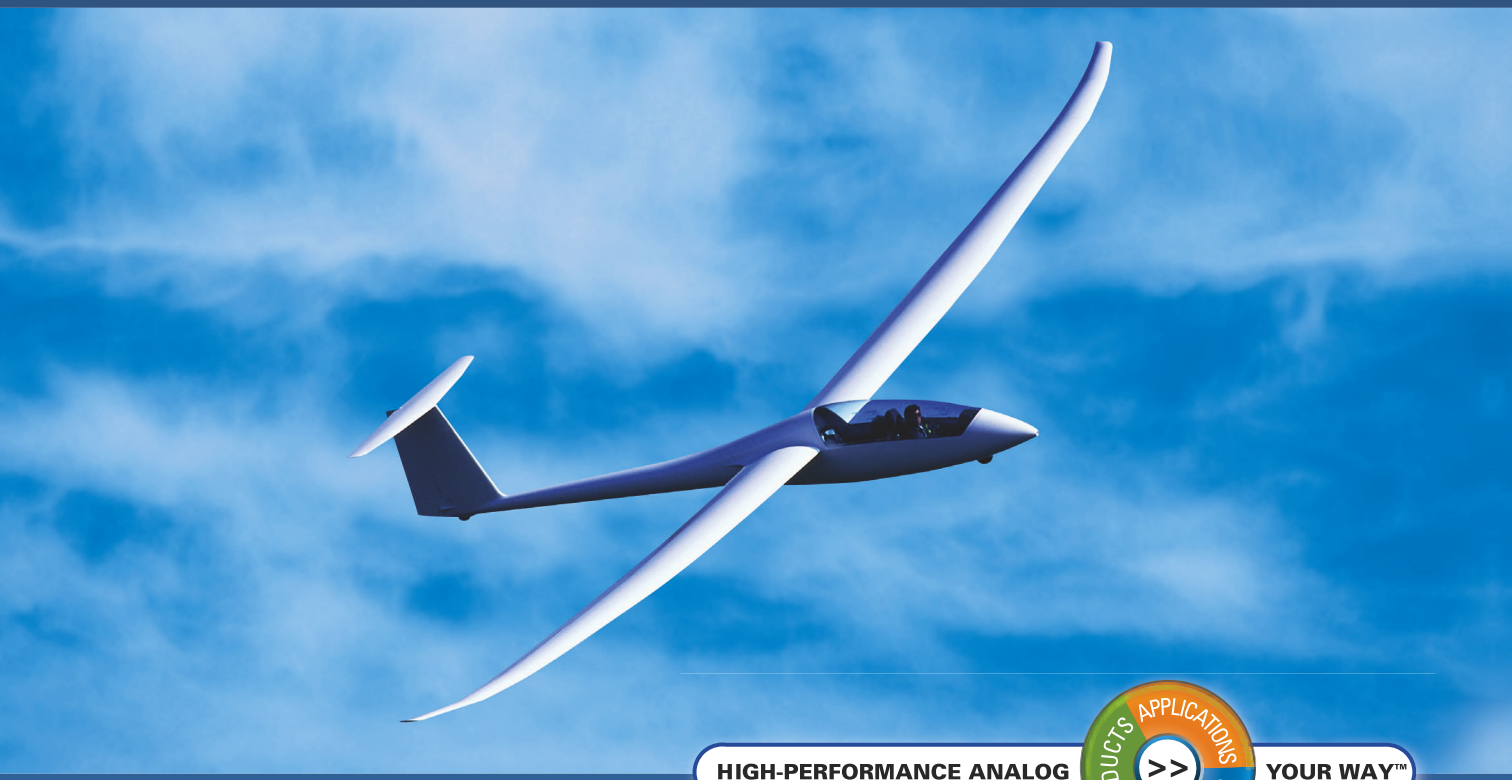
Lower Power, Higher Performance

1µA, 1.8V, Zero-Crossover Op Amp



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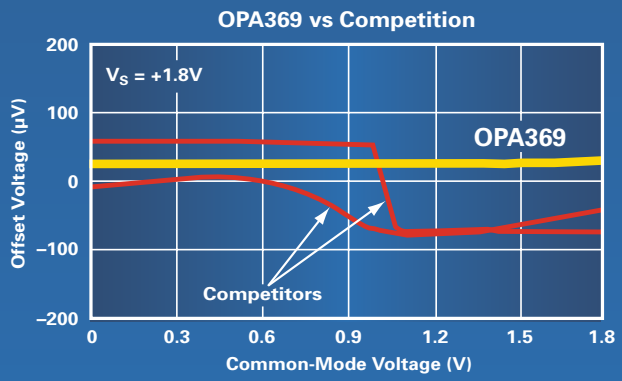

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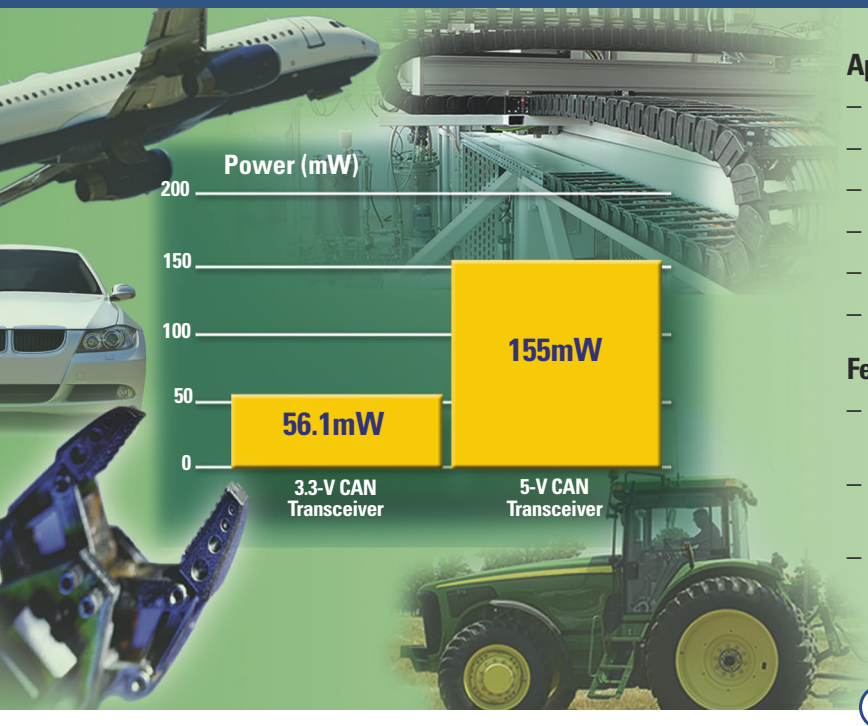

Applications

- Industrial automation
- Low-power battery applications
- DeviceNet, CANopen, Safety BUS
- SAE J1939 truck, bus, construction interface
- NMEA 2000 and SeaTalk2 Marine interface
- ISOBUS ISO11783 agricultural interface

Features

- Industry-leading ESD on bus pins delivers reliability in harsh environments
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Device	I/O and V_{CC} Levels (V)	Short-Circuit Protection (V)	ESD (kV)	Supply Current (mA)	Stand-By Current (µA)	Features
SN65HVD230	3	–4 to +16	16	17	370	Low-Power Standby
SN65HVD231	3	–4 to +16	16	17	0.04 Sleep	Ultra-Low-Power Sleep
SN65HVD232	3	–4 to +16	16	17	NA	Economical
SN65HVD233	3	–36 to +36	16	6	200	Standby, Diagnostic Loopback
SN65HVD234	3	–36 to +36	16	6	200/0.05 Sleep	Standby, Ultra-Low-Power Sleep
SN65HVD235	3	–36 to +36	16	6	200	Autobaud Loopback; Standby
SN65HVD251	5	–36 to +36	14	14	<275	Low-Power Standby
SN65HVD1040	5	–27 to +40	12	10	5	Low-Power Standby with Bus Wake-Up, Dominant Time-Out
SN65HVD1050	5	–27 to +40	8	6	NA	Listen-Only Mode, Dominant Time-Out

Parts shown in red are newly released

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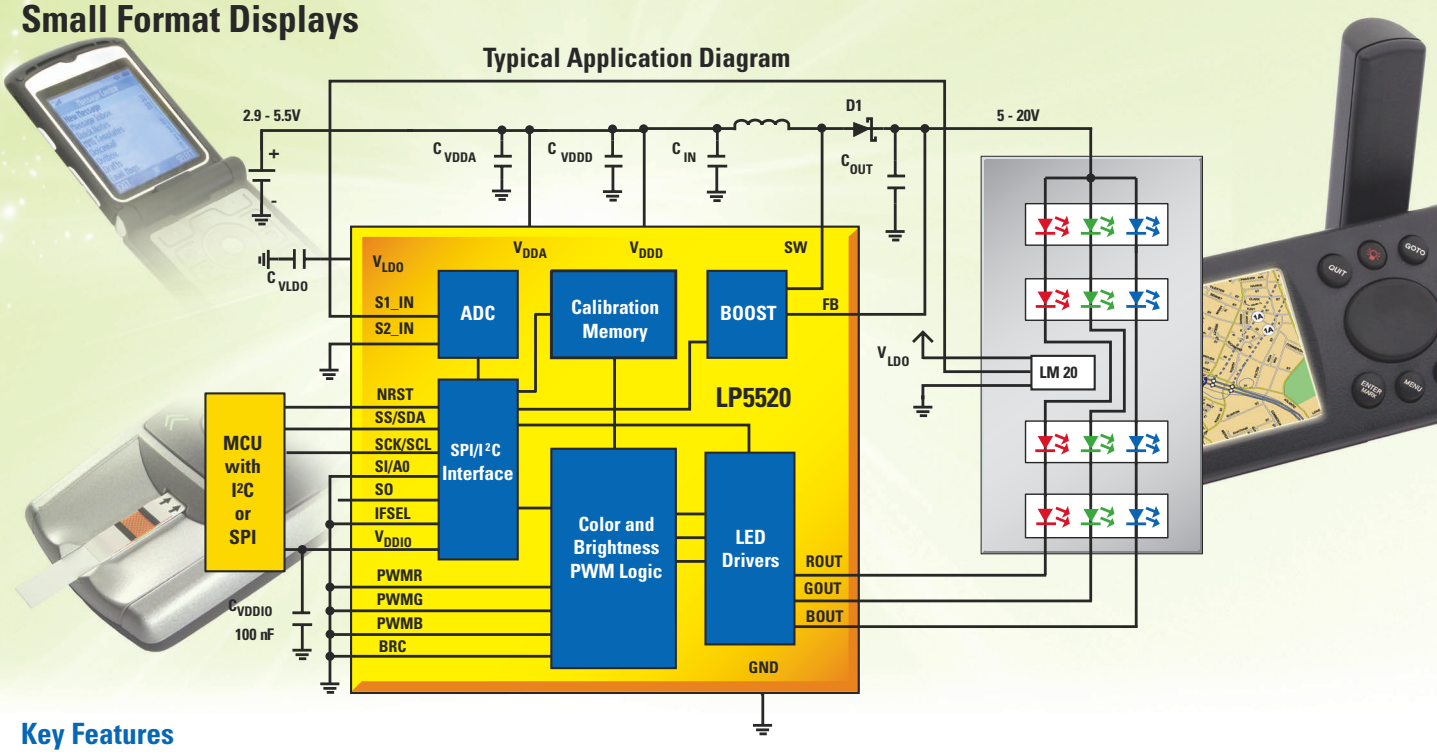
RGB LED Driver Generates Highly Efficient "True White" Backlighting

LP5520 Provides Innovative, Easy-to-Use, Instant Color Gamut Improvement for Small Format Displays



Key Features

- Temperature compensated LED intensity and color
- Individual calibration coefficients for each color
- Color accuracy ΔX and ΔY ≤ 0.003
- 100% NTSC color gamut, brighter color, better picture quality
- User programmability for effects, aging, dimming
- PWM control inputs for each color

Product	Description	Packaging
NEW! **LP5520**	RGB Backlighting LED driver with integrated white balance compensation	microSMD-25
NEW! **LP5521**	Programmable, low power, 3-channel LED driver	microSMD-20, LLP-24
NEW! **LP5522**	Autonomous single LED controller with one wire interface	microSMD-6
LP5526	Lighting Management Unit with high voltage boost converter with up to 150 mA serial flash LED driver	microSMD-25
LP5527	LED driver for camera flash and 4 LEDs with I²C programmability, LED connectivity, test, and audio synchronization	microSMD-30
NEW! **LP55281**	13 channel LED driver with audio sync, LED connectivity test and independent PWMS/PWMS blinking cycles	microSMD-36

Ideal for navigation systems, mobile phones, medical devices, and other portable devices

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9.13.07

Distributed linear regulators increase output current and spread the heat

 Parallel-board layout and heat spreading provide designers new ways to use linear regulators in all-surface-mount approaches. These techniques work well in today's high-performance, high-density PCBs.

by Robert Dobkin, Linear Technology Corp

How low can you go? A look at 45-nm-IC-design challenges

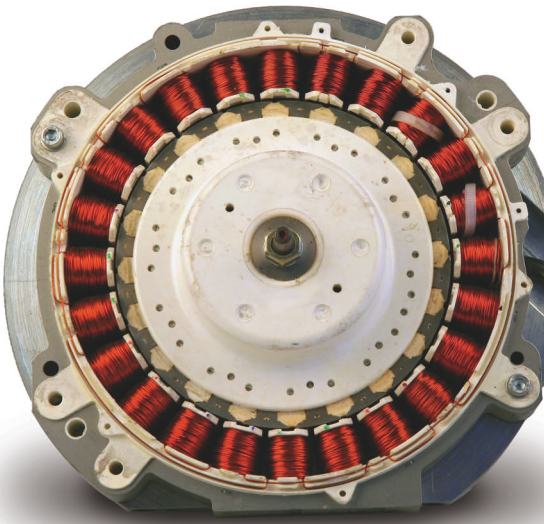
 If you have tools for the 65-nm or even the 90-nm node, moving to the 45-nm node requires no retooling. But designers moving to this node must adopt some advanced design techniques and be aware of some new design rules that foundries have imposed to ensure that SOC designs yield acceptable results.

by Michael Santarini, Senior Editor

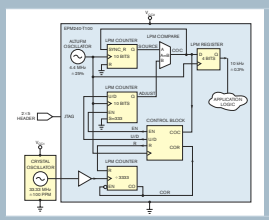
Permanent-magnet motors boost efficiency and power density

 Sensorless versions of these highly efficient motors reduce cost and parts count, but the motors still require complex control algorithms. Match the right motor type and controller to your application for the best performance and cost.

by Margery Conner, Technical Editor

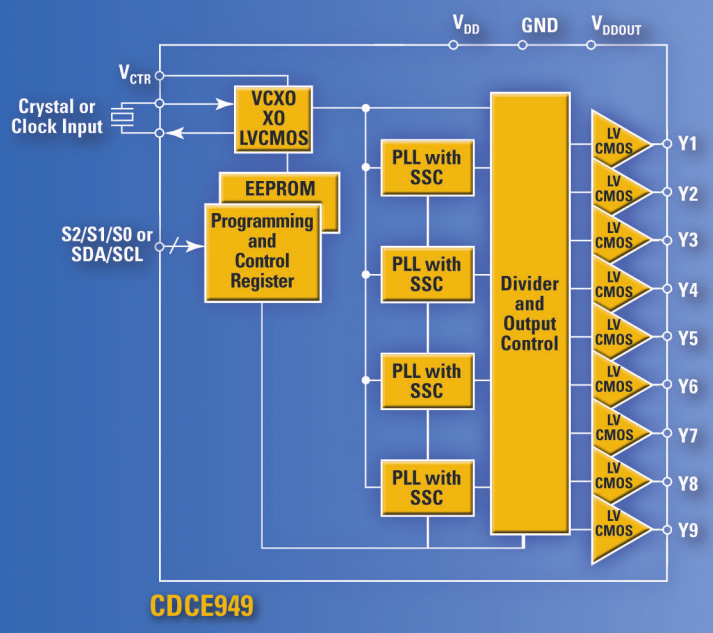


DESIGNIDEAS



Flexible Clock Generators

Multiple I/O-V and Programmability Ease System Design



Applications

– Digital media systems (audio/video)
– IP-STB/TV/phone
– Streaming media (DVD-P/R)
– GPS receivers
– Portable media and printers
– TI DSP, OMAP™ and DaVinci™ media processors

Features

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– 1 to 4 PLLs
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– I^2C and EEPROM programmability
– On-chip Voltage Controlled Crystal Oscillator (VCXO)
– 14-, 16-, 20- and 24-pin TSSOP

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Texas Instruments produces a portfolio of low-power, low-jitter, programmable clock generators capable of generating up to nine output clocks from a single input frequency – each output is programmable in-system for any clock frequency up to 230MHz. This level of functionality provides the system designer with capabilities previously unavailable in clock/timing products.

Device	Supply Voltage (V)	I/O Voltage (V)	# of PLL	# of Outputs	Output Frequency (MHz)	Temperature Range (°C)	Package (TSSOP)
CDCE949	1.8	2.5/3.3	4	9	230	–40 to +85	24
CDCE937	1.8	2.5/3.3	3	7	230	–40 to +85	20
CDCE925	1.8	2.5/3.3	2	5	230	–40 to +85	16
CDCE913	1.8	2.5/3.3	1	3	230	–40 to +85	14
CDCEL949	1.8	1.8	4	9	230	–40 to +85	24
CDCEL937	1.8	1.8	3	7	230	–40 to +85	20
CDCEL925	1.8	1.8	2	5	230	–40 to +85	16
CDCEL913	1.8	1.8	1	3	230	–40 to +85	14

Part shown in red is newly released

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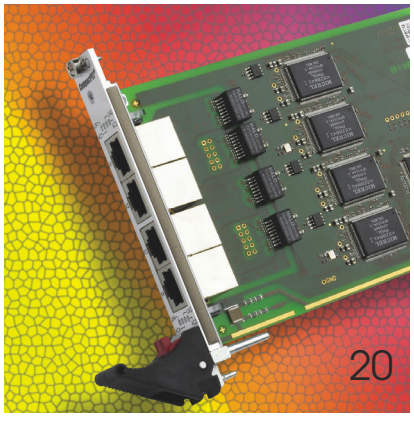

DEPARTMENTS & COLUMNS

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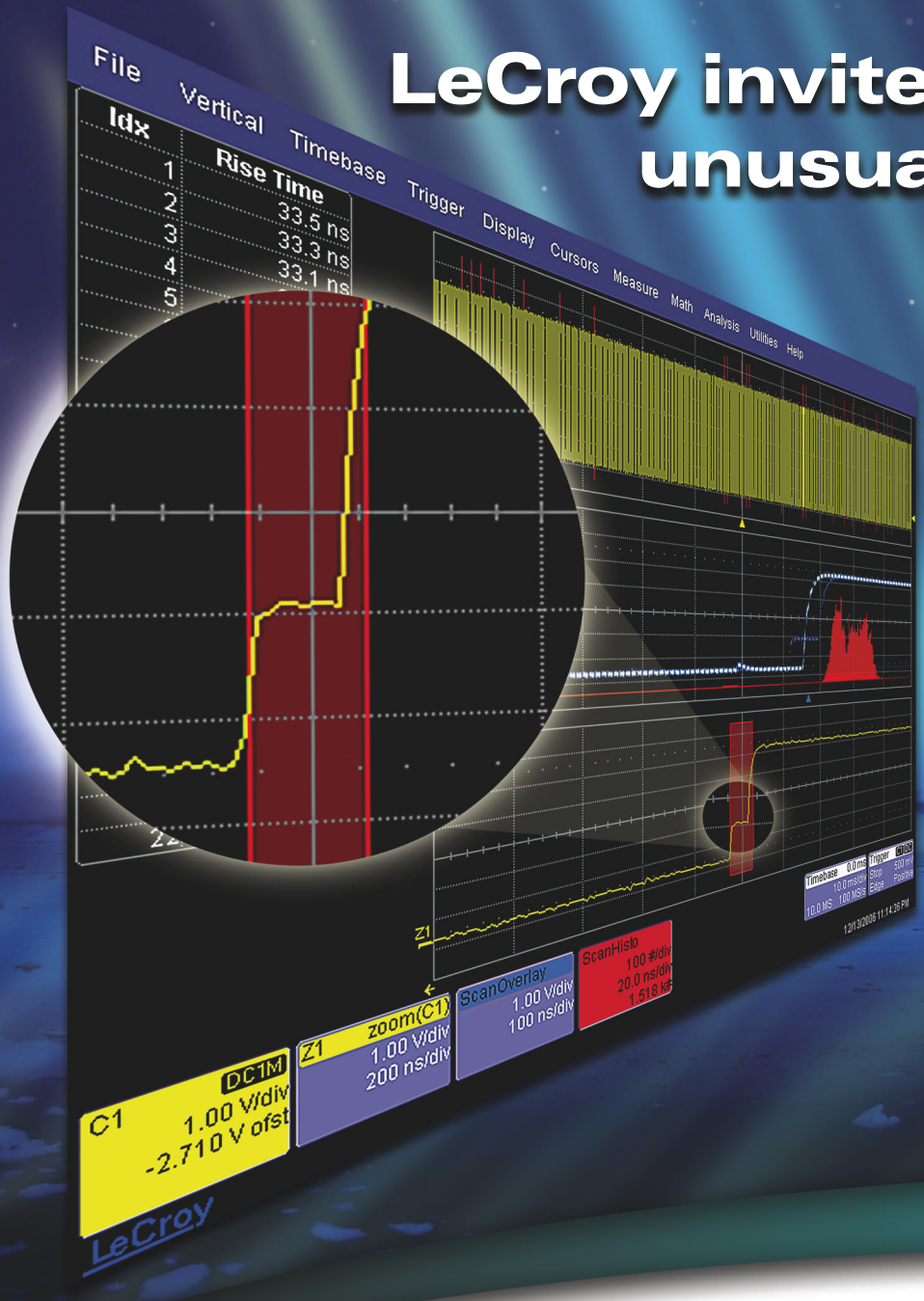

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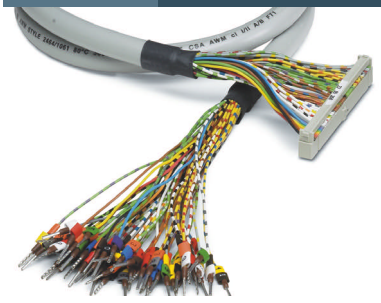

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BY MAURY WRIGHT, EDITORIAL DIRECTOR

PCB prototypes add value in the design process

I spend a good portion of my time meeting with companies in the EOEM (electronics-original-equipment-manufacturing) market, and most of those meetings are with semiconductor vendors due to the vast number of such companies. But on a recent trip to the Northwest, I spent time with some different types of companies—two of which are involved in the prototype-PCB (printed-circuit-board) area. The meetings got me thinking about how engineers use prototype PCBs in the design process. I'll offer up a few things I heard. I'm also hoping that you will respond in the Feedback Loop comment section located alongside the online version of this article and tell us and your fellow readers how you use prototype PCBs.

First, I met with LPKF Laser & Electronics (www.lpkfusa.com). LPKF makes equipment that allows design engineers to quickly make their own prototype PCBs. A number of years ago, *EDN* ran a feature on this technology that you might find interesting: See www.edn.com/article/CA45861. LPKF offers computer-controller PCB plotters along with milling machines and plating systems. For as little as $10,000, you can buy the gear you need to build PCB prototypes, although the price can escalate based on your needs for multilayer and SMT (surface-mount-technology) support. The company even offers laser-based plotters for small production runs.

LPKF President Stephan Schmidt claims that design engineers drive the purchase of most of the company's systems due to the need for building prototypes during the design process. Schmidt doesn't suggest that techniques such as simulation aren't valuable. But he claims that designers often yield higher quality and better performing systems when they can do a series of prototypes to test the system architecture and design.

I would have guessed that most designers ordering prototype PCBs would not order the PCB in the target-system form factor.

Even if you don't have an immediate need for a prototyping system in your lab, you might still want to request a copy of the LPKF catalog. In the back of the catalog, the company offers a technical guide on PCB manufacturing. Although the catalog presents the information relative to LPKF products, there is also good general information, including sections on design for microwave and RF systems and on SMT designs. LPKF is also worthy of praise for its efforts to encourage engineering education. The company provides refurbished gear to high-school pre-engineering programs.

Later in my trip, I met with Sunstone Circuits (www.sunstone.com), a manufacturer that specializes in prototype PCBs. Originally, Sunstone was in the production-PCB business, but almost all of the production-PCB business has moved to Asia. Sunstone allows designers to specify and order PCBs online and often can deliver products in two days. The company also offers free PCB-design software.

I would have guessed that most designers ordering prototype PCBs would not order the PCB in the target-system form factor. I'm accustomed to seeing reference designs and development boards with extra connections that offer access to interconnects between chips and to test ports. But Sunstone claims that 80 to 90% of its orders are in the target-system form factor. Rocky Catt, Sunstone's executive vice president and chief operating officer, claims that some designers will build prototype PCBs with more layers than the production board will use. For the prototype, the designer might rely on an autorouted layout that could lead to extra layers, whereas for the production board, the designer will hand-optimize the board to minimize the number of layers.

How do you use prototypes? Do you prototype only challenging parts of a system design? Do you iteratively build prototype PCBs to tune a design? How should *EDN* cover PCB design? Are we delivering information you need? You can certainly e-mail me or call me with answers, but by posting your comments online, your fellow readers can benefit from your thoughts as well. EDN

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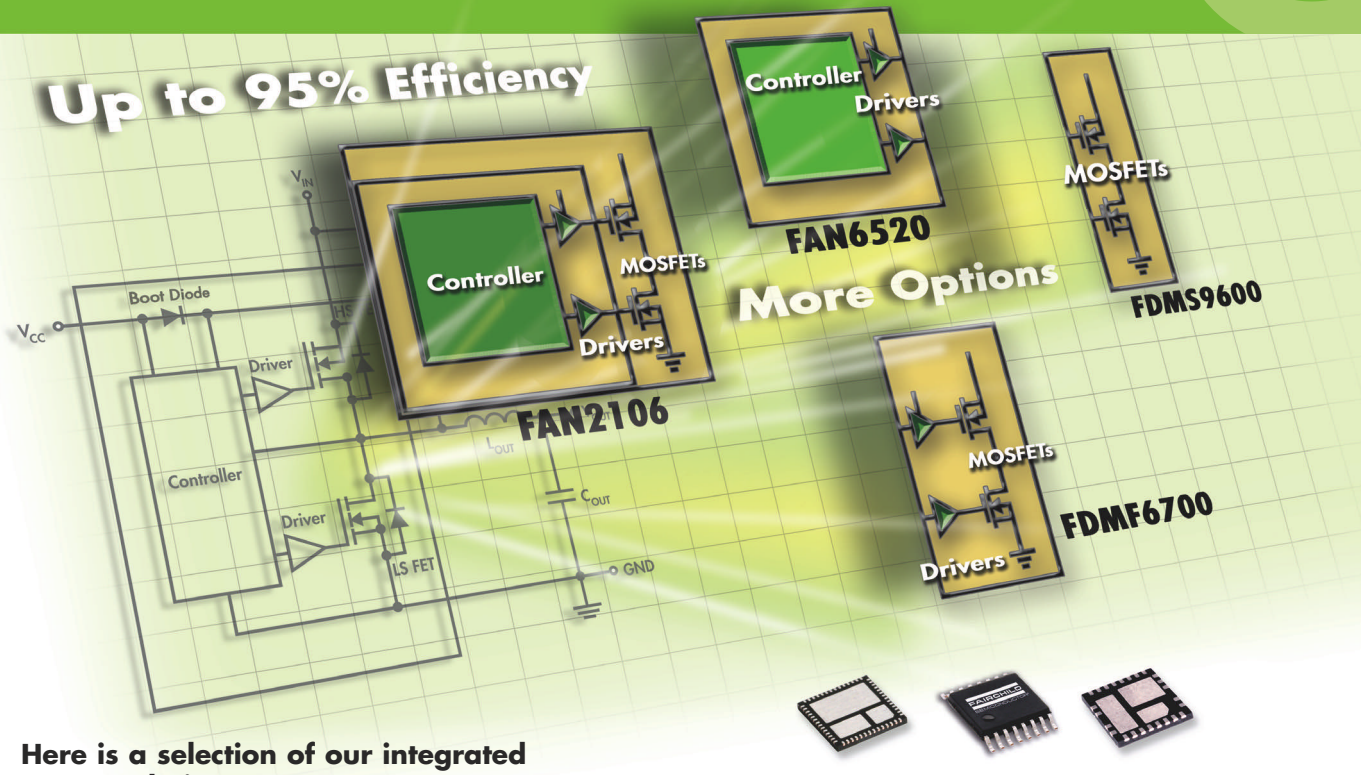

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Power Controllers (Controller + Drivers)	FAN6520	• Drives N-Channel MOSFETs in a synchronous buck topology • Output voltage range as low as 0.8V to V_{IN}
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Integrated MOSFETs (multiple MOSFETs in one package)	FDMS9600 FDMS9620	• 50% board space savings versus discrete solution • Ease of layout in PCB design • Optimized matching and sizing of MOSFETs (>92% efficiency) • MLP 5×6 package

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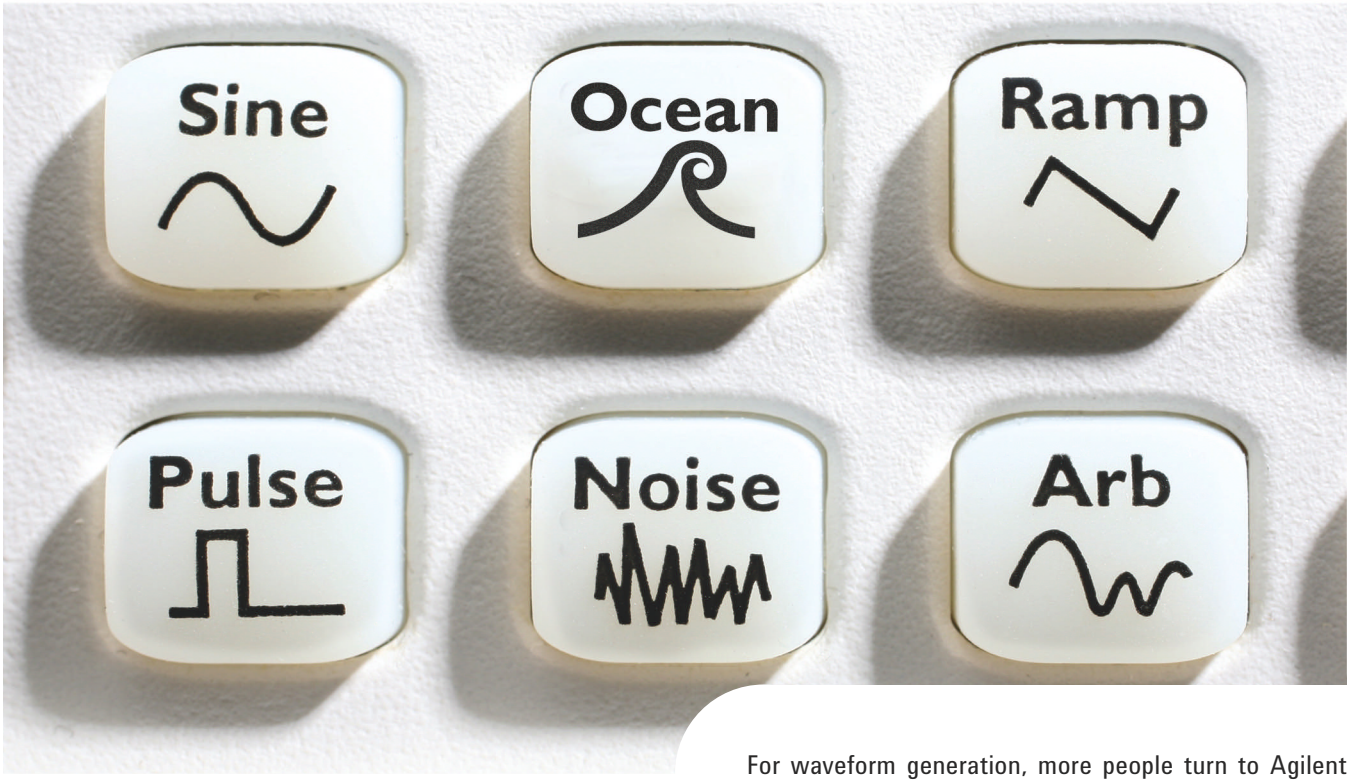

Agilent 33220A Function Generator

	33220A *20 MHz Sine & Square*	***33250A*** *80 MHz Sine & Square*
Basic Waveforms	*11 Built-in Low Distortion*	
Pulse	*Variable Edge 5 MHz*	*Variable Edge 50 MHz*
Arbitrary Waveforms	*14-bits, 64K points*	*12-bits, 64K points*
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Agilent Technologies has announced the U2000 Series of USB-based 9-kHz to 24-GHz power sensors, which are smaller, lighter, and less expensive than typical power meters and similar power-sensing instrumentation. Because the new sensors operate without power meters or extra hardware modules, they save bench space and simplify RF-power measurements in crowded work areas. The sensors work with a variety of Agilent spectrum analyzers and network analyzers and thus extend those instruments' abilities to make accurate average-power measurements. In addition to fast and easy setup with plug-and-play USB connectivity, the sensors, in combination with the N1918A Power Analysis Manager software, also simplify monitoring and troubleshooting. Because the USB-powered sensors provide built-in triggering, they require no external power adapters or triggering modules for synchronization with external instruments or events.

> "With the rising need for multiple-channel power measurements in various industries, these power sensors are the affordable, simple solution that our customers have requested."

"The USB sensors' ability to operate without a power meter marks a breakthrough in our offerings for power measurements," says Ee Huei Sin, vice president and general manager of Agilent's Basic Instruments Division. "With the rising need for multiple-channel power measurements in various industries, these power sensors are the affordable, simple solution that our customers have requested."

According to Gooi Soon Chai, vice president and general manager of Agilent's Electronic Instruments Business Unit, the highly portable units demonstrate Agilent's commitment to providing affordable, reliable, and continually improved test-and-measurement products. The series includes four models that deliver as many as 250 readings/sec and a −60 to +20-dBm power range. Each sensor includes a high-speed USB 2.0 interface for simple, quick setup. With internal zeroing capability, calibration does not require disconnecting the sensor from the device under test, hence reducing test time and sensor wear and tear.

With the N1918A Power Analysis Manager software, the sensors display power-measurement results on a PC or another appropriate instrument. In addition to the normal waveform-monitoring option, the software eases monitoring and troubleshooting through functions such as limit and alert settings, record and playback, multiple-list view, overlay, and channel mathematics. Prices starts at $2300.

—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com/find/usbsensor_pr.

The U2000 Series USB-powered RF-power sensors are small, fast, light, and—except for the results display, which you see on a host computer—complete. The single small module replaces a conventional sensor and a power meter. With a conventional sensor, the meter not only displays the measurement results, but also supplies power to the sensor and conditions the sensor's output.

FEEDBACK LOOP

"Surface-mount jacks make no sense. I've resoldered my share (and not because I'm careless). All it takes is a drop with the plug still in, and buh-bye to connection."

—Reader Dan Kingsbury speaks out, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6447234. Add your comments.

Video-codec cores offer programmability

As more and more devices—from cell phones to surveillance cameras to robots—require video capture, video codecs are becoming almost standard building blocks for SOCs (systems on chips). Given the complexity of the computing tasks involved, this area might appear to be one in which specialized hardware will reign unchallenged. But an Aug 13 introduction from ARC International disputes that idea.

ARC, a long-standing vendor of customizable RISC cores, has argued for years that properly augmenting a RISC core with SIMD (single-instruction/multiple-data) execution engines enables that core to handle tasks well beyond the range of a CPU alone. The company supports this argument with a family of—for now—five video-codec subsystems, each comprising an ARC 700 RISC core, one or more SIMD units, and specialized hardware.

The advantage of putting the heavy-lifting burden onto programmable hardware is flexibility. These new ARC VRaptor cores come with supporting software for H.263, H.264, MPEG-4, JPEG, VC-1, and a variety of other codecs. They are adaptable to custom applications, such as the H.264/video-analytics blends that are starting to find use in video surveillance. The disadvantage of the programmable approach, traditionally, has been high power consumption for relatively low performance. And, although advanced processes and aggressive power management have to some degree mitigated this problem, physics issues remain. Accordingly, high-end performance for the cores in this family is H.264 Base Profile, D1-resolution encoding at 30 frames/sec.

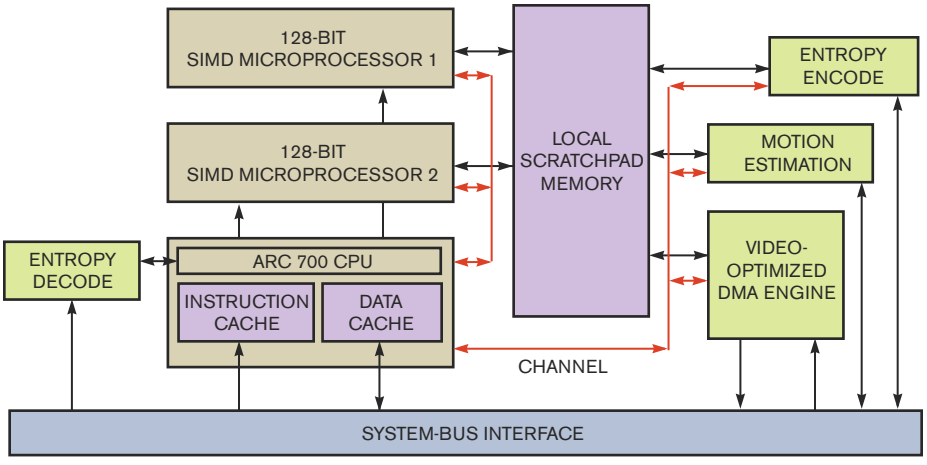
You must use this benchmark with some care, however, because you can speed things up in a software-driven codec by disabling procedures that improve picture quality or reduce bit rate. Conversely, if you turn on all the bells and whistles for excellent picture quality, you can slow down the encoder operation. And power increases with clock frequency and activity, so the more bells and whistles, the more milliwatts the system consumes. For this and other reasons, ARC quotes power-consumption figures only under a nondisclosure agreement.

The underlying hardware for the high-end core includes a 700-series RISC CPU core, local memory, a sophisticated DMA arrangement, two SIMD units, and special hardware blocks for motion encoding and for entropy encoding and decoding. The SIMD units are extensions of ARC's standard SIMD engine, with additional instructions for dealing with video-processing tasks. The specialized units are dedicated hardware blocks with some degree of programmability to accommodate differences in codec requirements. In operation, the RISC core handles sequencing and control, and the SIMD engines take on the high-bandwidth tasks, such as pixel-level transforms and deblocking.

ARC estimates that the high-end 417V core will be slightly larger than 10 mm², including all internal-RAM structures, in TSMC's (Taiwan Semiconductor Manufacturing Co, www.tsmc.com) 130g process, using Cadence's (www.cadence.com) layout flow and Virage Logic (www.viragelogic.com) libraries. Engineers have extensively simulated the cores and verified them in FPGA emulation, and they are available now. For more on these products, see "Video codecs in software: some reflections on programmable-hardware approaches," www.edn.com/070913p1.

—by Ron Wilson

▷**ARC**, www.arc.com.

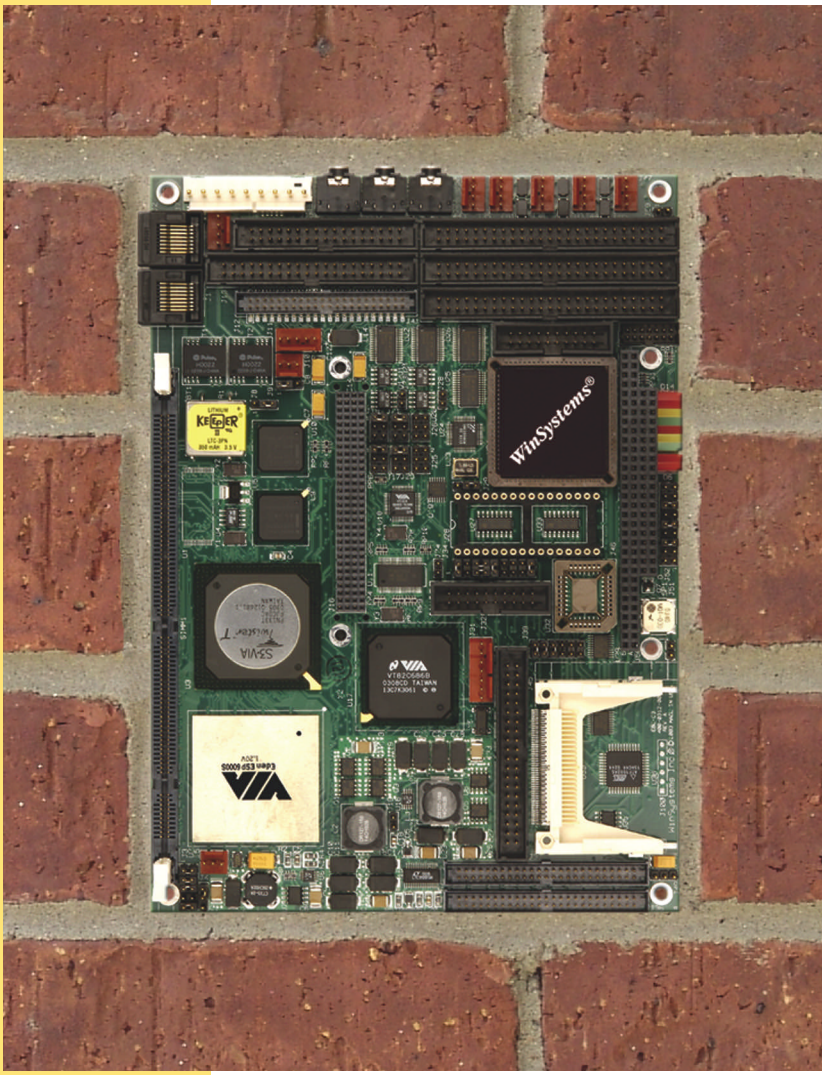


VRaptor combines an ARC RISC core with both programmable and fixed-function units.

DILBERT By Scott Adams

BUILT TO LAST

Fanless EBX 733MHz P3 with COM, dual ENET, USB and Video



- VIA 733MHz or 1GHz C3 CPU
- PC-compatible, supports Windows® XP, CE, Linux and x86 RTOS
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- Up 1GB bootable DOC®, 512KB SRAM, or 1MB EPROM
- Type I and II CompactFlash cards supported up to 8GB
- CRT, flat panel, and LVDS
- Two 10/100 Ethernet controllers
- Four USB ports
- Four serial COM ports
- LPT, Kybd, and mouse
- 48 bi-directional I/O lines
- Two EIDE and one floppy disk controller
- AC97 Audio supported
- PC/104 & PC/104-*Plus* expansion
- +5 volt only operation
- EBX size: 5.75" x 8.0" (146 mm x 203 mm)
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- Quick Start Developers Kits for Windows® XP, CE, and Linux
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The EBC-C3 embeds 9 different functions to provide a processor- and I/O-intensive solution. It operates over a -40° to +85°C temperature range without the need of a fan, making it ideal for embedded applications such as robotics, MIL/COTS, transportation, pipeline, and machine control.

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Extended Temperature

Cadence and Mentor create free, open-source SystemVerilog methodology

In an effort to make it easier for users to create interoperable SystemVerilog verification flows, Cadence Design Systems and Mentor Graphics have jointly created and are announcing that they will standardize on the free, open-source OVM (Open Verification Methodology). Steve Glaser, corporate vice president of marketing in the verification division at Cadence, and Dennis Brophy, director of strategic-business development at Mentor, say that each EDA vendor offering SystemVerilog simulation flows has so far developed its own guidelines. Users must adopt these guidelines to develop verification IP (intellectual property) for their flows. Mentor has offered the AVM (Advanced Verification Methodology), and Mentor has offered the UVM (Unified Verification Methodology).

"Our customers have noticed that we've continued down this path of using our own proprietary, company-centric methodologies because they have to support N number of ways of doing things on N×N number of tools, which is making their job of porting verification information a challenge," says Brophy. "What we have been doing is hampering design collaboration."

Today, for example, a user could develop a piece of VIP (verification IP), such as a SystemVerilog testbench or a transaction-level or RTL (register-transfer-level) model using one vendor's format, but that VIP might not easily work in the other vendor's SystemVerilog simulation environment. "Users would essentially have to do the work themselves and build a bridge between the two vendors' environments to make the VIP work in the other's tool environment," says Brophy. "The new OVM will eliminate the need for users to create that bridge on their own. We are enabling a truly interoperable VIP environment, promoting language interoperability and enabling data portability across multiple simulator platforms to deliver on the promise of SystemVerilog and open up a healthy and vibrant design-and-verification community."

> "The new methodology is a direct competitor and a competitive response to Synopsys' proprietary VMM SystemVerilog guidelines.

The new OVM is a superset of AVM and UVM, and Cadence and Mentor each dedicated developers to combine the best of both worlds to create OVM. The OVM deliverables include the OVM Methodology, which comprises how-to documentation, examples, and code snippets, and an OVM class library—essentially the building blocks to develop VIP.

Glaser and Brophy say that the OVM will allow customers and third-party providers of VIP to create testbenches and models in one format that will run in any OVM-compliant tool environment. "We tried to look at this problem quite holistically and said that to enable this methodology, we had to standardize on an open set of functional building blocks, called class libraries. But there are a lot of methodological implications that then connect into even higher-level library functions and even into the way that tools need to interpret data and the way that customers need to take IP from different sources and configure it for different parameters. They then start operating it, controlling it, and being able to get messages back," says Glaser. "There are a lot of considerations for plug-and-play IP from multiple sources as well as the path from block to chip to system-level reuse, which tends to bring in other languages such as SystemC." Brophy and Glaser claim that OVM addresses all those issues and fully complies with the IEEE OpenVerilog language standard 1800-2005.

At least initially, the new methodology is a direct competitor and a competitive response to Synopsys' (www.synopsys.com) proprietary VMM SystemVerilog guidelines, which also comply with IEEE 1800-2005. Synopsys has been a proponent of SystemVerilog and, some would say, the front-runner in the market ever since a few years ago when it acquired Co-Ware Design Automation, the company that originally developed SystemVerilog. But the VMM, say Glaser and Brophy, has been less than open and has lacked significant links into SystemC. (Industry participants viewed SystemVerilog and SystemC as competing languages when they debuted a few years ago.) However, both Brophy and Glaser claim that Synopsys has in the past declined to join any open SystemVerilog efforts. Synopsys and all other vendors are free to adopt the OVM at any point, and broad adoption of a single viable SystemVerilog methodology would help users use their multivendor SystemVerilog-tool flows and would likely increase the use and general sales of SystemVerilog tools and methods. "We think OVM will be a great step toward speeding up the adoption of SystemVerilog and advanced verification methodologies," says Glaser.

Both companies had to modify their SystemVerilog simulation environments so that they could run VIP created using the OVM guidelines. Both companies have verified that their simulation platforms, Mentor Questa and Cadence Incisive, can run VIP created with the OVM guidelines. Brophy notes that making the tools OVM-compliant wasn't a painstaking process, so it should be fairly easy for other vendors to make their tools OVM-compliant.

The companies are offering the free OVM as the Apache 2.0 open-source license. The companies will initially offer it to selected customers in the third quarter of this year and plan to make the production release, which includes the methodology and supporting library, in the fourth quarter of this year. Initially, Apache 2.0 will be available for downloading from Cadence's and Mentor's Web sites, but plans are in the works to eventually make it available from a dedicated Web site.

—by Michael Santarini

▷**Cadence Design Systems**, www.cadence.com.

▷**Mentor Graphics**, www.mentor.com.

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Processor lowers the cost and power thresholds for HD video

The TMS320DM355 processor is the latest addition to Texas Instruments' DaVinci processor family. Unlike previous DaVinci devices, this processor does not include a software-programmable DSP. Rather, it couples an ARM936EJ-S core with a video-processing subsystem and MPEG-4 JPEG coprocessor that are configurable through software executing on the ARM core. The less-than-$10 processor enables HD (high-definition)-video products, such as digital cameras and IP (Internet Protocol) videocameras targeting a $250 end-unit price, as well as digital-photo frames and video baby monitors targeting a $120 end-unit price. Going with a configurable hard coprocessor instead of a software-programmable DSP helps the system deliver power consumption as low as 400 mW to support HD MPEG-4 encoding and approximately 1 mW in standby; this power-consumption level allows for 80 minutes of continuous HD-video capture with two AA batteries.

The processor supports HD MPEG-4 SP encoding or decoding at 720p and 30 frames/sec and JPEG encoding or decoding at 50M pixels/sec. It is available in 216- or 270-MHz clock speeds; these devices support only these rates because the video subsystem and coprocessor blocks operate at the same clock rate as the processor. The video-processing subsystem is the same set of engines that all DaVinci devices feature. The processor supports the same intellectual-property and API (application-programming-interface) model as the other DaVinci devices. It includes production-qualified, configurable HD MPEG-4 and JPEG codecs without licensing fees or royalties. The peripheral suite includes a high-speed USB 2.0 OTG (On-The-Go) device and mini-host with a PHY (physical) layer, a 10-bit DAC, 32 kbytes of program/data memory, 8 kbytes of ROM, 16- and 8-kbyte instruction and data caches, and an external memory interface that supports mobile DDR/DDR2.

The DM355 is available for sampling now in a 13×13-mm, 329-pin, 0.65-mm-pitch BGA package. The 216-MHz device sells for $9.75 (50,000), and the 270-MHz device sells for $11.49 (50,000). The TMDX-EVM355 evaluation module is available now for $495. It includes JPEG/MPEG-4 SP/G.711 codecs, ORCAD schematics, and MontaVista Linux with drivers for the peripherals, video-processing subsystems, and Uboot loader.

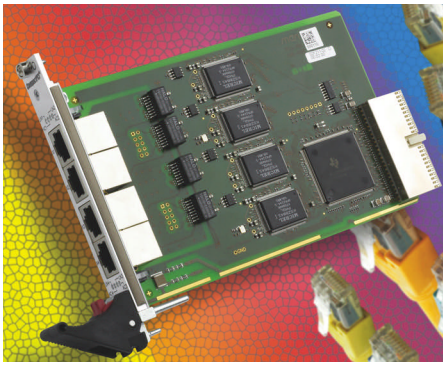
—by Robert Cravotta

▷**Texas Instruments**, www.ti.com.

Module controls four network channels

A new 3U CompactPCI network controller from MEN Micro offers four fast Ethernet ports for control of multiple network configurations, including firewalls, gateways, routers, and fieldbus-data concentrators. The single-slot F211 controller features four full- or half-duplex channels that support 10BaseT and 100BaseTX physical layers and provide autonegotiation, collision, and link detection with a maximum data transfer of 200 Mbps. Each of the four channels has a unique MAC/IP (media-access-control/Internet Protocol) address, enabling the F211 to function in a redundant mode when you use the lines in parallel for high-availability systems. For harsh and mobile applications, the 32-bit, 33-MHz F211 operates over an extended temperature range of −40 to +85°C. The controller comes with software drivers for the Windows, Linux, QNX, and VxWorks operating systems. Price for the F211 is $544, and delivery is within six weeks.**—by Warren Webb**

▷**MEN Micro Inc**, www.men.de.



The F211 network controller features quad fast Ethernet channels for flexible control of multiple network configurations.

REFERENCE DESIGN PREVENTS POWER THEFT

09.13.07

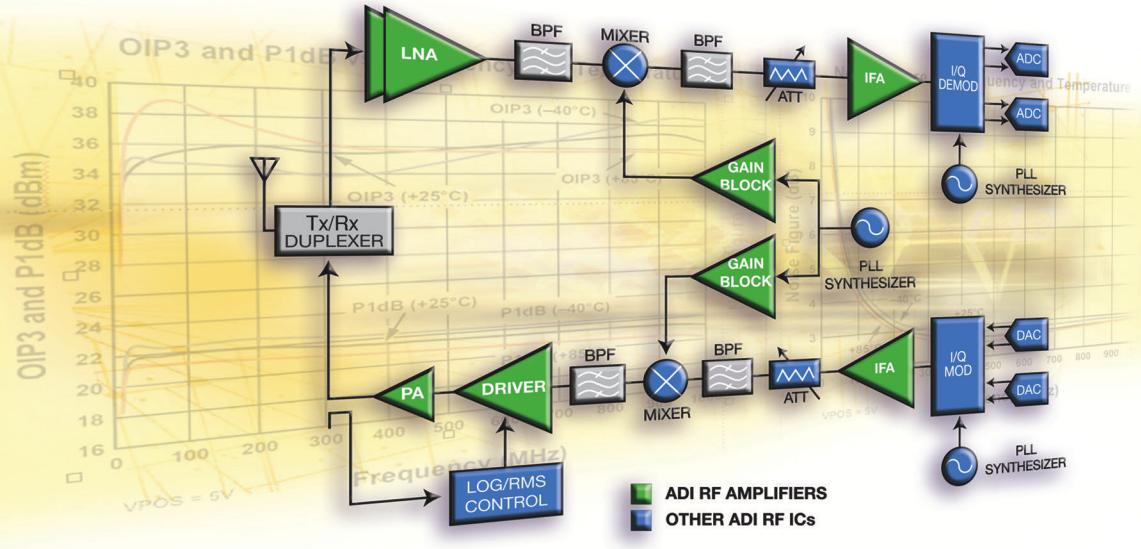
Some people respond to the high cost of energy by stealing it. To prove that fact, Metering.com recently published a report showing that, in some countries, tampering with meters accounts for 5% of illegally consumed electricity. That tampering doesn't happen just in Third World countries, either: The report estimates that losses in the United States are approximately 4%. According to Silvestro Fimiani, product-marketing manager for the company, the most common way to disable meters is to use a large permanent magnet to provide an intense external magnetic field.

Energy thieves can saturate an electricity meter's transformer core with a large permanent magnet.

Addressing this problem, Power Integrations has published a reference design based on its LinkSwitch XT family. The design, for an isolated power supply in flyback configuration, delivers 150 mA at 5V, and an external magnetic field does not affect it. It also consumes just 1W and produces the regulated 750 mW that advanced meter electronics require.—by Margery Conner

▶**Power Integrations, www.powerint.com.**

The highest performance RF amplifiers. Across the signal chain, analog is everywhere.



Low Noise Amplifiers (LNA)

Part Number	Freq Range (MHz)	Gain (dB)	OIP3 (dBm)	P1dB (dBm)	NF (dB)	Current (mA)	Specs @ (MHz)	Price
ADL5521	400 to 4000	15.3	35.3	22.5	0.8	65	1950	$2.15
ADL5523	400 to 4000	17.5	33.7	21.9	1.0	65	1950	$2.15

Intermediate Frequency Amplifiers (IFA)

Part Number	Freq Range (MHz)	Gain (dB)	OIP3 (dBm)	P1dB (dBm)	NF (dB)	Current (mA)	Specs @ (MHz)	Price
ADL5530*	DC to 1000	16.8	37.0	21.8	3.0	110	190	$1.56
ADL5531	20 to 500	20.3	40.9	20.7	2.7	101	190	$2.25
ADL5532	20 to 500	16.1	39.1	19.7	3.0	95	70	$2.25
ADL5533 (75 Ω)	30 to 1000	19.8	37.3	18.7	2.9	66	70	$2.55
ADL5534 (Dual)	20 to 500	19.8	41.8	20.0	2.5	90	70	$3.29

Gain Blocks

Part Number	Freq Range (MHz)	Gain (dB)	OIP3 (dBm)	P1dB (dBm)	NF (dB)	Current (mA)	Specs @ (MHz)	Price
AD8353*	1 to 2700	19.5	22.8	8.3	5.6	42	900	$0.48
AD8354*	1 to 2700	19.5	19.3	4.8	4.4	25	900	$0.48
ADL5541	50 to 6000	14.7	39.2	16.3	3.8	92	2000	$1.65
ADL5542	50 to 6000	18.7	39.0	18.0	3.2	92	2000	$1.65

Driver Amplifiers

Part Number	Freq Range (MHz)	Gain (dB)	OIP3 (dBm)	P1dB (dBm)	NF (dB)	Current (mA)	Specs @ (MHz)	Price
ADL5320	400 to 2700	13.7	42.0	25.6	4.2	104	2140	$2.55
ADL5322	700 to 1000	19.9	45.3	27.9	5.0	320	900	$3.48
ADL5323	1700 to 2400	19.5	43.5	28.0	5.0	320	2140	$3.48

*3 V bias is also supported.

All prices shown are $U.S. in 1k quantities unless otherwise noted.

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ANALOG DEVICES

RESEARCH UPDATE

BY RON WILSON

Los Alamos lab makes major step in quantum-dot lasers

Victor I Klimov, PhD, leads a team at Los Alamos National Laboratory that has been working for a number of years on turning NQDs (nanocrystal quantum dots) into lasers. Because the dots are so small, their size influences the energy gap between the conduction and the valence bands. When the recombination of an electron-hole pair causes the release of light in a laser, the color of the light relates to the energy gap. Hence, Klimov and company could change the color of an NQD laser simply by fabricating larger or smaller dots—if they could get the NQDs to be lasers.

However, for reasons that again relate to the size of the dots, you must have more excited electrons than valence-band electrons in a dot to get light amplification. An incoming photon hits one excited electron, an action causing the emission of a photon. However, if you don't excite most of the valence electrons, odds are that the next unexcited electron will just absorb the emitted photon. You might think the solution is just to excite more of the electrons, but there is a problem with this approach, too.

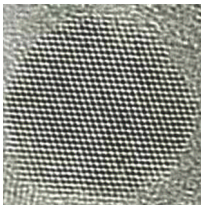
Again because of quantum effects, electron-hole pairs and neighboring electrons interact to recombine quickly in NQDs—too quickly to permit laser action and without releasing a photon. Recently, however, Klimov and his team have reported that, by fabricating nanocrystals with a cadmium-sulfide core surrounded by a zinc-selenide shell, the physical interface separates the conduction-band electrons from the corresponding holes in the valence band, substantially slowing recombination and making light amplification possible. A conceivable result could be nanosized, color-to-order lasers for sensing and optical interconnect.

▷**Los Alamos National Laboratory**, www.lanl.gov.

Silicon nanocrystals promise 40% solar-cell efficiency

A research team at the NREL (National Renewable Energy Laboratory) claims to have observed production of two to three electrons from a single photon in a silicon nanocrystal. The result is potentially highly significant for the photocell business. Scientists had previously thought that silicon could produce only one excited electron per photon—limiting the conversion efficiency of silicon photocells without the aid of light-concentrating hardware to approximately 20 to 30%.

Previously, other researchers had observed multiple-electron production in exotic materials, but these substances offered little hope of production in the volumes necessary to impact the world's growing energy needs. The NREL work, in contrast, used ordinary silicon. The trick is that these researchers confined the silicon into nanocrystals. The fact that the size of the crystal approaches atomic scale means that the behavior of subatomic particles, such as electrons, in the material can fundamentally differ from their behavior in the same material in bulk.



A 7-nm chunk of crystalline silicon could dramatically increase the efficiency of solar cells.

Some questions about the methodology remain, because researchers can only indirectly observe electron production in photovoltaics of this type. And no one has contemplated mass production of large arrays of quantum dots. But nanocrystals of semiconductor material are relatively easy to produce through solution chemistry, so such problems may not turn out to be showstoppers. The payoff could be commercial photovoltaic panels with as much as 40% unaided efficiency.

▷**National Renewable Energy Laboratory**, www.nrel.gov.

NANOSTRUCTURES ENABLE PAPERLIKE SUPERCAPACITORS AND BATTERIES

09.13.07

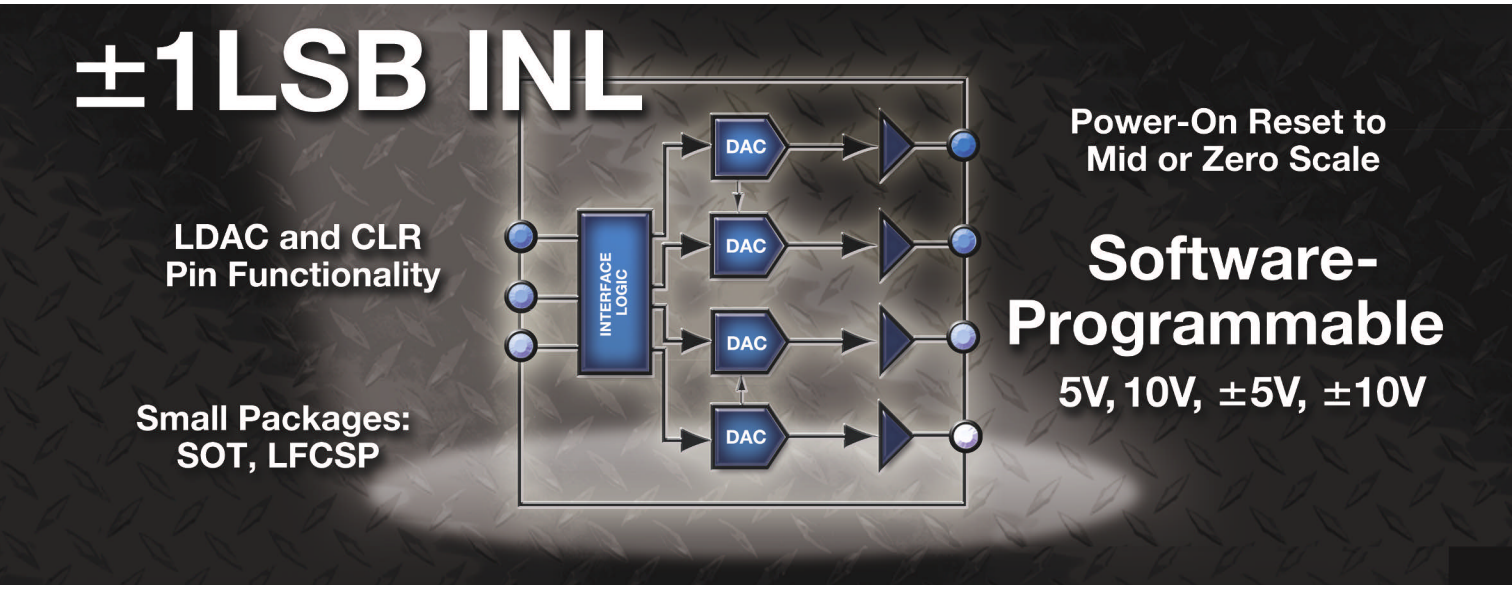
The carbon nanotube has made another appearance in the literature, this time giving researchers quite a charge. Researchers at Rensselaer Polytechnic Institute have reported the use of the structures in creating a family of thin, paperlike batteries and supercapacitors.

The researchers observe that batteries, capacitors, and devices that combine those functions in application-specific ways all rely on the same three elements: an electrode material, a dielectric material, and a nonreactive matrix to support the other two. Starting from this conceptual basis, the researchers created a thin matrix of cellulose fibers–essentially, a very clean sheet of paper. They then developed a technique for diffusing carbon nanotubes into the paper in a way that leaves the tubes aligned with each other. The resulting structure acts as a very-low-effective-resistance electrode with an enormous effective surface area. By then diffusing a nonaqueous electrolyte into the sheet of paper, the sheet can become a battery, a capacitor, or a combination of the two, depending on the choice of electrolytes and the patterns in which you diffuse them.

The whole structure retains its paperlike characteristics. You can twist, roll, fold, or stack it to make multicell batteries or capacitors, and you can trim it to shape, all without destroying its electrical properties. In addition, because all three materials behave well over temperature, batteries using the structures can operate over a very wide temperature range. The researchers' paper appeared in the Aug 15, 2007, *Early Edition of the Proceedings of the National Academy of Sciences* (www.pnas.org).

▶**Rensselaer Polytechnic Institute, www.rpi.edu.**

More 16-bit DAC performance for more designs. In process control, analog is everywhere.



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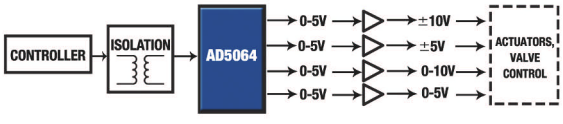

AD5754
Flexible Solution for Closed-Loop Systems

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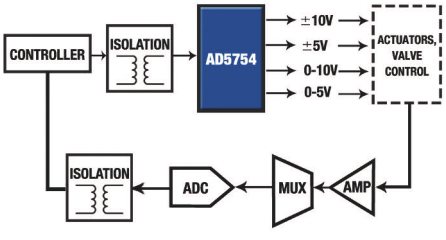

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Part No.	Description	Price
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AD5065	Dual, 5 V, ±1 LSB INL (max), 2.3 mA @ 5 V	$11.25
AD5064	Quad, 5 V, ±1 LSB INL (max), 5 mA @ 5 V	$15.95
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BY GARY GIUST, PHD

Jitter peaking and PLLs

My audiophile brother prizes his tube transistors and vinyl-record collection. It doesn't bother him that every pass of the metal needle on vinyl creates friction that slowly degrades his records' fidelity. Engineers creating clock trees by cascading several PLL (phase-locked-loop) chips may relate to this situation. Jitter peaking with each PLL acts as a "needle" that degrades the timing of the input signal, or "record." As this signal passes through subsequent PLLs, jitter peaking can accumulate to cause instability or timing failures. **Figure 1a** shows a worst-case scenario in which a chosen PLL with significant peaking connects three times in series, causing this peaking to accumulate. The first question to ask in this situation may be surprising: Is jitter peaking really a problem?

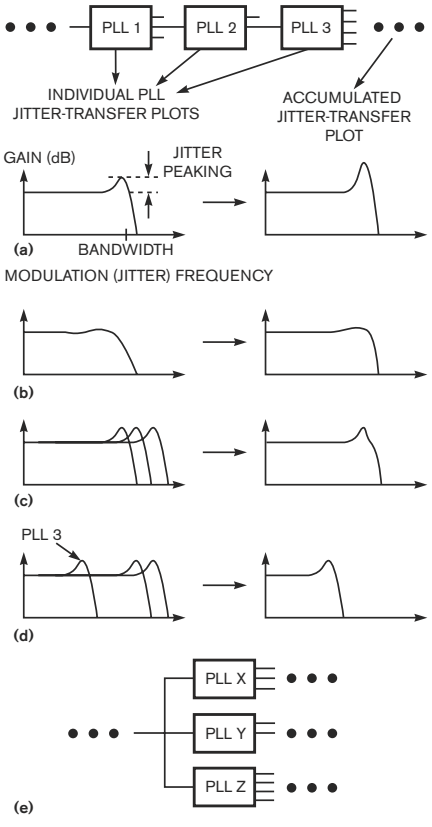


Figure 1 Cascading three identical PLLs amplifies jitter peaking (a). Avoid this problem by selecting overdamped PLLs (b), three different PLLs (c), the lowest bandwidth for the last PLL (d), or an alternative clock tree (e).

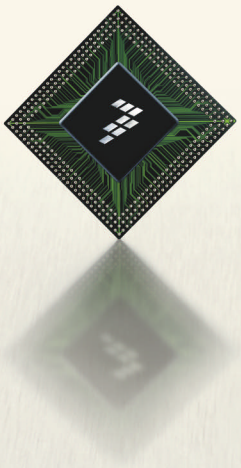
Just because jitter peaking exists doesn't mean there is a problem. First, consider the application. Most PLLs exhibit some degree of peaking—typically, 3 dB—and not all applications require the tightest timing margins. At the other extreme, architectures based on cascaded regenerators cannot permit jitter peaking to accumulate unbounded. For example, SONET (synchronous-optical network) specifies less-than-0.1-dB peaking. Another way to analyze this issue is to ask: What signals and noise are present in the system? If there is no frequency content in which jitter peaking occurs, then this peaking has little impact on system performance, assuming that the PLL is stable. In other words, if the needle wears a groove in the "vinyl" that you cannot hear or, in my brother's case, feel, then there is little impact.

What if jitter peaking *is* a problem? One approach cascades only PLLs having overdamped loops common in applications such as SONET (**Figure 1b**). However, this approach increases cost and limits chips selection. **Figure 1c** shows an approach that avoids using identical PLLs more than once in any clock-tree path. Because each PLL has a different bandwidth, the frequencies at which peaking occurs are staggered, making it difficult for peaking to compound. If multiple vendors act as second sources for the same chip, use each vendor's chip once rather than the same vendor's chip many times, because each company uses different process technologies and design approaches, causing the peaking to occur at different frequencies. When using spread-spectrum clocking to reduce EMI (electromagnetic interference), make sure each PLL's bandwidth is wide enough to pass the spread modulation.

Another approach doesn't restrict how you cascade PLLs, except that the last PLL has the lowest bandwidth of all devices in its path. **Figure 1d** shows that jitter attenuator PLL 3 filters any peaking that accumulates in the tree. However, because PLL 3 is averaging—not tracking—the input-phase error from this peaking, make sure that the PLL can tolerate any worst-case expected phase errors so that it remains locked at all times.

The simplest approach avoids cascading PLLs altogether, in which jitter peaking in any path depends on only one device (**Figure 1e**). When this approach is impossible, request jitter peaking data in decibels and hertz from potential vendors to help understand the impact of cascading their devices and in choosing your available options. EDN

Gary Giust, PhD, is a marketing manager at PhaseLink Corp. He also conducts seminars on jitter. Contact him at gary@jittertime.com.



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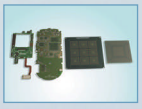

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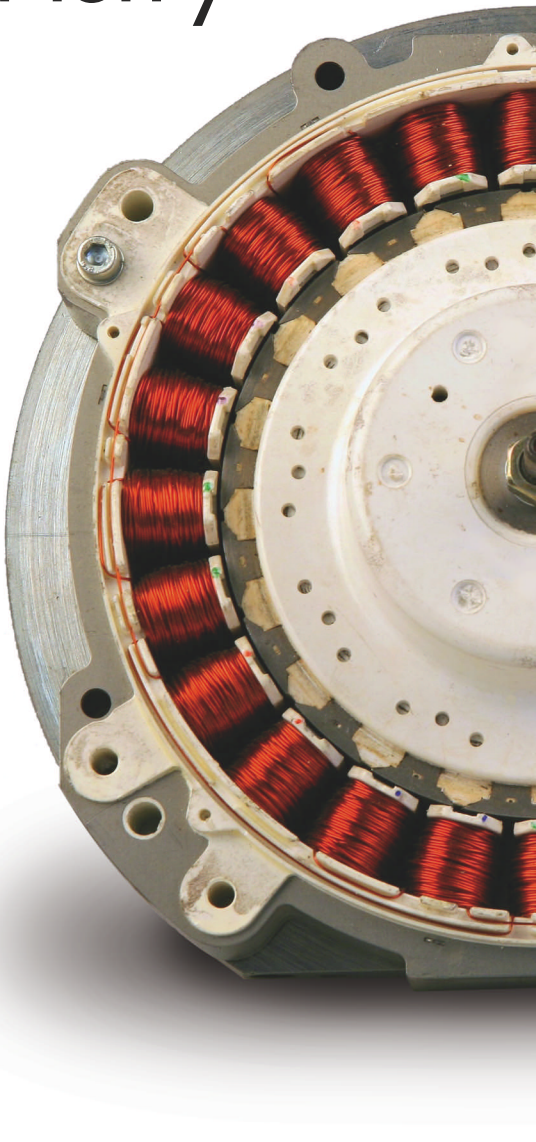
PERMANENT-MAGNET MOTORS boost efficiency and power density

BY MARGERY CONNER • TECHNICAL EDITOR



The global price of energy is at an all-time high, with few signs of relief in sight, making consumers and businesses alike interested in energy conservation. Currently, the most common motor type in use is the single-phase ACIM (ac-induction motor), which is efficient only while running at a constant speed, though most applications—whether in the home or in industry—run at variable speeds. Worse, applications with a reverse speed, such as washing machines, require gearboxes, which reduce power density as well as efficiency. For high-power applications, using ACIMs is still the rule, but, at 2 kW and less, permanent-magnet motors are taking over in new designs. (As a reference, a washing-machine motor uses about 1 kW or less.)

Permanent-magnet motors have been commercially available since the '90s but didn't initially see widespread use because of the high cost that they owe to the expensive permanent magnets on their rotor. In addition, their complex control algorithms require specialized engineering expertise as well as the additional expense of an embedded processor (see **sidebar** "How permanent-magnet motors work" at the Web version of this article at www.edn.com/070913df).

Recently, however, the price of copper, which both the stator and the rotor windings of ACIMs use, has risen. These prices have had less impact on permanent-magnet motors, which lack rotor windings. At the same time, permanent-magnet prices have dropped.

At their most basic, permanent-magnet motors require some kind of sensor—usually, a Hall-effect type—to determine the position of the rotor with respect to the windings on the stator. The motor's control-drive electronics use the rotor-position feedback to adjust the pulse-width-modulated drive signals to the windings. However, using sensors is not the only way for the control electronics to monitor position: Motor-control processors have become more powerful and can now calculate rotor position from the motor's back EMF (electromotive force), eliminating the need for position sensors for some applications (**Figure 1**). For example, new designs for hermetically sealed refrigeration compressors are moving to perma-

nent-magnet motors for higher power efficiency. Formerly, they relied on single-phase ACIMs, which required just two electrical connections through the hermetic seal. It's not a big leap for the designs to bring out one more line for a three-phase permanent-magnet motor drive, but bringing out three additional position-sensor lines through the hermetic seal would be too expensive and decrease reliability. Sensorless permanent-magnet motors are better options.

However, sensorless permanent-magnet motors are not the answers for all applications. The rotor must be moving at some minimum speed to generate a back EMF, which sensing requires. These devices are good only for motors in applications whose operating speed ranges from 5 to 100% of the top speed. In addition, applications requiring precise positioning usually require sensored motors. But, for applications such as consumer appliances and many industrial-control systems, sensorless permanent-magnet motors are making significant inroads.

There are two kinds of permanent-magnet motors: brushless-dc motors and PMSMs (permanent-magnet synchronous motors). Brushless-dc-motor windings give a trapezoidal back EMF and respond to a trapezoidal-drive signal (**Figure 2a**); PMSMs produce a sinusoidal back EMF and require a sinusoidal-drive signal (**Figure 2b**). Their different drive signals and, thus, their torque make for a key difference in the drive characteristics of the two motors: The brushless-dc motor is subject to torque ripple of approximately 13%, and the PMSM theoretically has 0% torque ripple.

A six-step commutation process drives brushless-dc motors. As the process applies the drive voltage between two phases of the windings, the third phase senses the back EMF. The sequence to drive the rotor takes six steps; hence, manufacturers often call this sequence a six-step process. This algorithm is relatively straightforward, and you can implement it with an 8-bit processor or with an 8-bit processor and a hardware-based coprocessor. Freescale, Infineon, Microchip, STMicroelectronics, and Texas Instruments have developed the software for the six-step commutation algorithms for their microcontrollers and DSCs (digital-signal controllers), which are, in general, 8-bit devices.

AT A GLANCE

- Permanent-magnet motors are more efficient than ac-induction motors, but they require more sophisticated control circuitry.
- Sensorless permanent-magnet motors are less expensive and more reliable than those with sensors, but some applications that require less-than-5%-of-maximum speed or frequent stops and starts require sensors.
- Microcontroller, DSC (digital-signal-controller), and semiconductor vendors are offering development platforms with control algorithms to ease the task of designing for these motors.

FOC HELPS PMSMs

However, brushless-dc motors have drawbacks that make them unsuitable for some applications. For example, the dynamic response of trapezoidal control isn't optimal for washing machines, because the load changes both dynamically within a wash cycle and varies from load to load and selected wash cycle. Further, in a front-loading machine, the gravitational power works against the motor load when the load is on the top side of the drum. The sinusoidally driven PMSM with FOC (field-oriented control) can better handle dynamic-load changes, but it requires a more powerful processor to handle the vector computations (**Reference 1**).

FOC relies on two algorithms: The Clarke algorithm converts the stator-winding-phase currents from a three-axis vector to a two-axis vector, referenced to the stator. The Park transform then converts the two-axis currents into a rotating system, still relative to the rotor. Clearly, the computational power these transformations require is both complex and computationally inten-

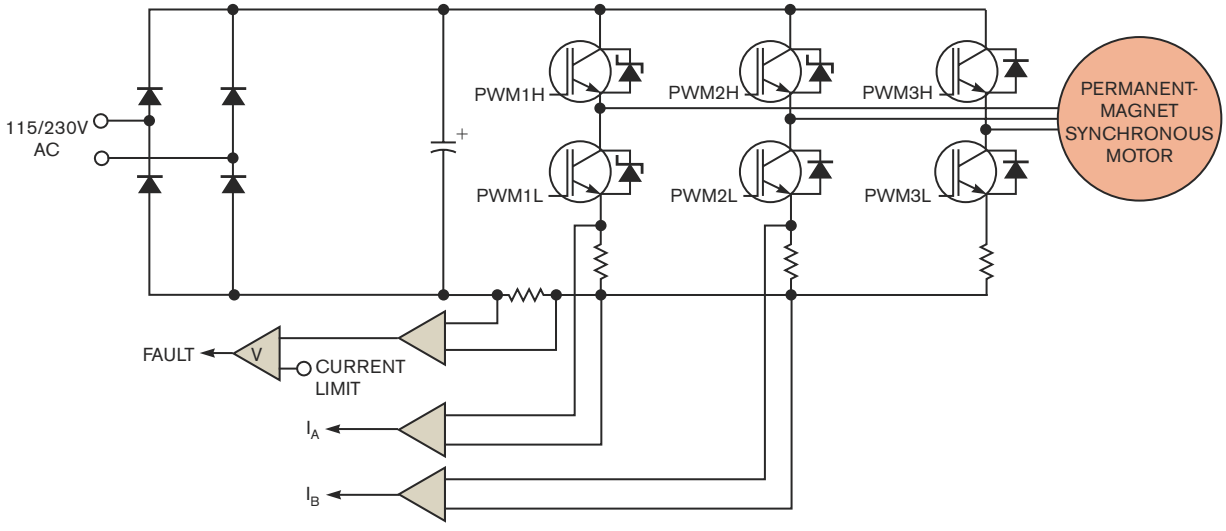


Figure 1 A three-phase permanent-magnet motor requires a processor to create the control algorithms for the inverter to drive the motor's windings. The six high and low PWM signals come from the motor-control processor. A sensorless permanent-magnet motor relies on the motor's back EMF to sense the rotor position and control the motor direction and speed. The processor uses currents I_A and I_B to calculate back EMF.

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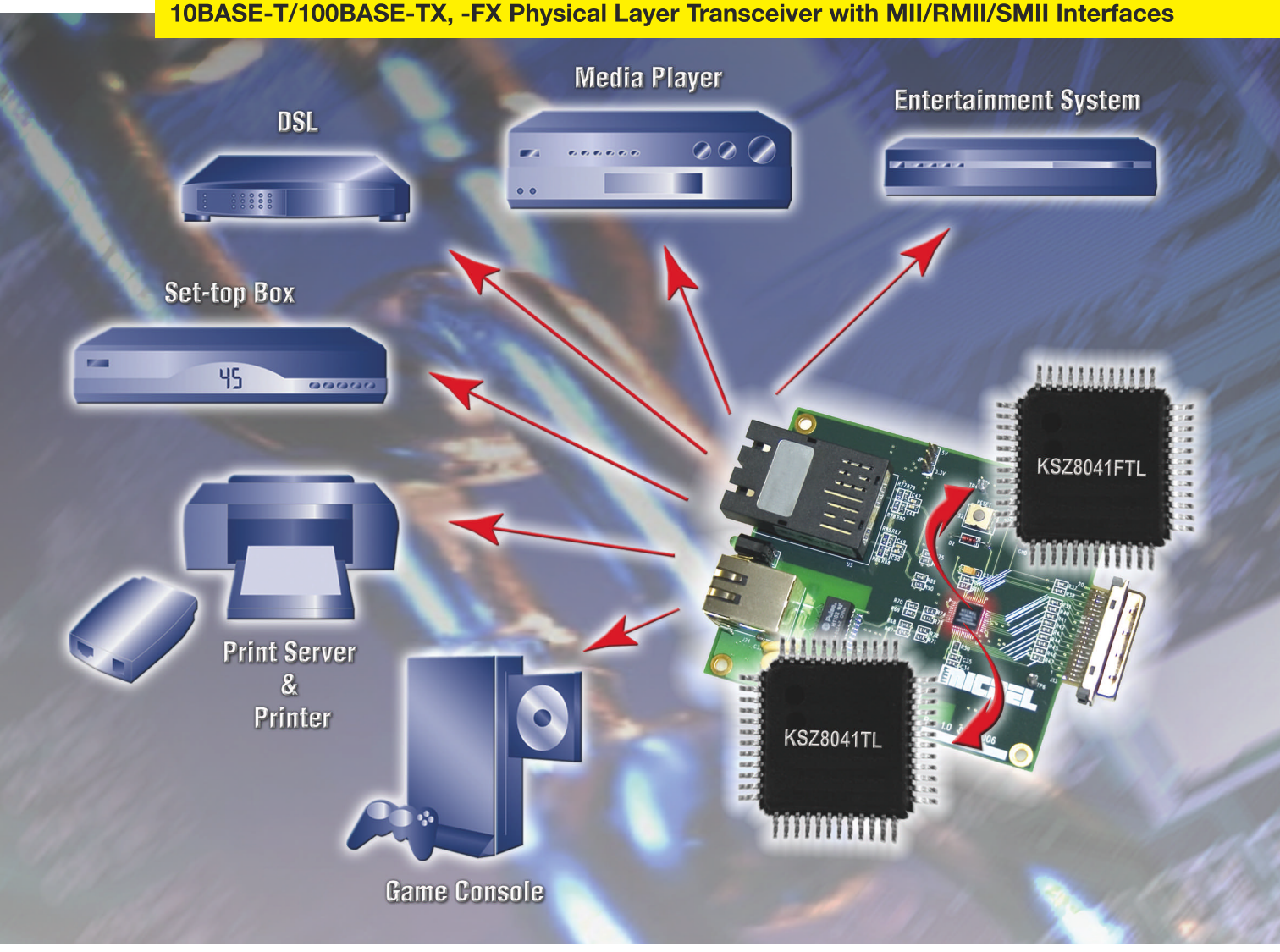

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sive. Several microcontroller and DSC vendors offer development platforms for their chips that they tailor to run these algorithms. Microchip offers the 16-bit dsPIC33FJ12MC201/203 DSC, which includes a PWM with two independent clock sources for advanced motor-control algorithms and active power-factor correction, as well as a user-selectable 1.1M-sample/sec, 10-bit ADC or 500k-sample/sec, 12-bit ADC. The DSC can operate at 40 MIPS, and the Clarke and Park algorithms require 11-MIPS performance, leaving 72% of the DSC's overhead for performing other tasks, such as computing power-factor control. The chips sell for $1.99 (volume quantities).

You can perform FOC-vector calculations with Infineon's 8-bit XC886/88 processor, which includes a CORDIC (coordinate-rotational-digital computer) to perform hard-coded trigonometric functions necessary for the Clarke and Park routines before transferring the result to the chip's general-purpose controller, which interfaces with the drive circuitry. The company offers FOC-software algorithms for the 8-bit processor that take up 58% of the CPU's performance. So, depending on what other chores your processor has, this amount of processing power could be enough. The 8-bit version sells for $2 to $3, depending on volume. Infineon plans to introduce a 16-bit version in October.

MORE AT EDN.COM

For a PowerSource blog post on algorithms and motor efficiency, see "As motors go green, free code helps to further reduce price," www.edn.com/070913df2.

For more on motor control, see "Inverters rev up small-motor drives" at www.edn.com/article/CA46852.

Go to www.edn.com/070913df and click on Feedback Loop to post a comment on this article.

These motor-controller engines all come from companies that are in the microcontroller business. These companies offer the algorithms in software that you can modify for performance in an application. International Rectifier's approach differs from these companies in that its iMotion platform implements the control algorithms in hardware, resulting in the usual hardware-versus-software-algorithm trade-off: The hardware algorithms run fast—with a typical FOC calculation taking just 11 µsec in the iMotion digital-control engine—but you can't modify them.

Freescale has teamed with Fairchild and Nidec Shibaura to make a package of Freescale's 56F800/E DSC family, Fairchild's switching-power semiconductors, and Nidec Shibaura's flat, round "pancake" PMSM; the initial products target washing machines. Freescale provides the sinusoidal-control algorithms for the motor controller, and Fairchild provides the high-power-semiconductor switches for the inverter-drive electronics. Nidec Shibaura's pancake motor tunes the DSC, inverter, and motor all to work with each other for the washing-machine application.

WATCH YOUR HEAD ROOM

Cliff Ortmeyer, market-development manager in the appliance sector for ST-Microelectronics, says that the 8-bit ST7MC1/2 processor dedicates a motor control to peripherals and works well for brushless-dc-motor control and the six-step control process. But he says that you need a more powerful 32-bit processor for the FOC of PMSMs. He agrees that it's vital to have adequate processing power in the controller to handle not only the vector computations, but also other system-control functions. "Our [PMSM-control] designs use less than 50% of the CPU to perform the main motor control. So, with the 32-bit ARM7/9 processor, that leaves a huge amount of power for the other application functions."

The price decreases and new technology for PMSMs make them inviting devices to employ, but they may not

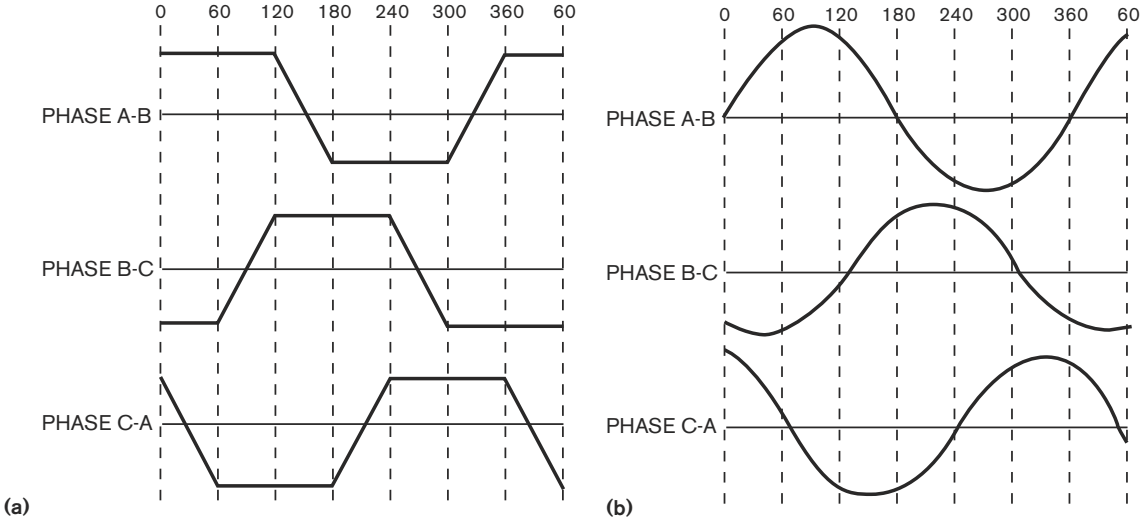

Figure 2 A trapezoidal-drive current in a six-step process drives a brushless-dc motor, possibly resulting in a torque ripple of as much as 13% (a). The motor-drive current to a PMSM is sinusoidal, giving an ideal torque ripple of zero, but the trade-off is that the control algorithm is more complex (b).

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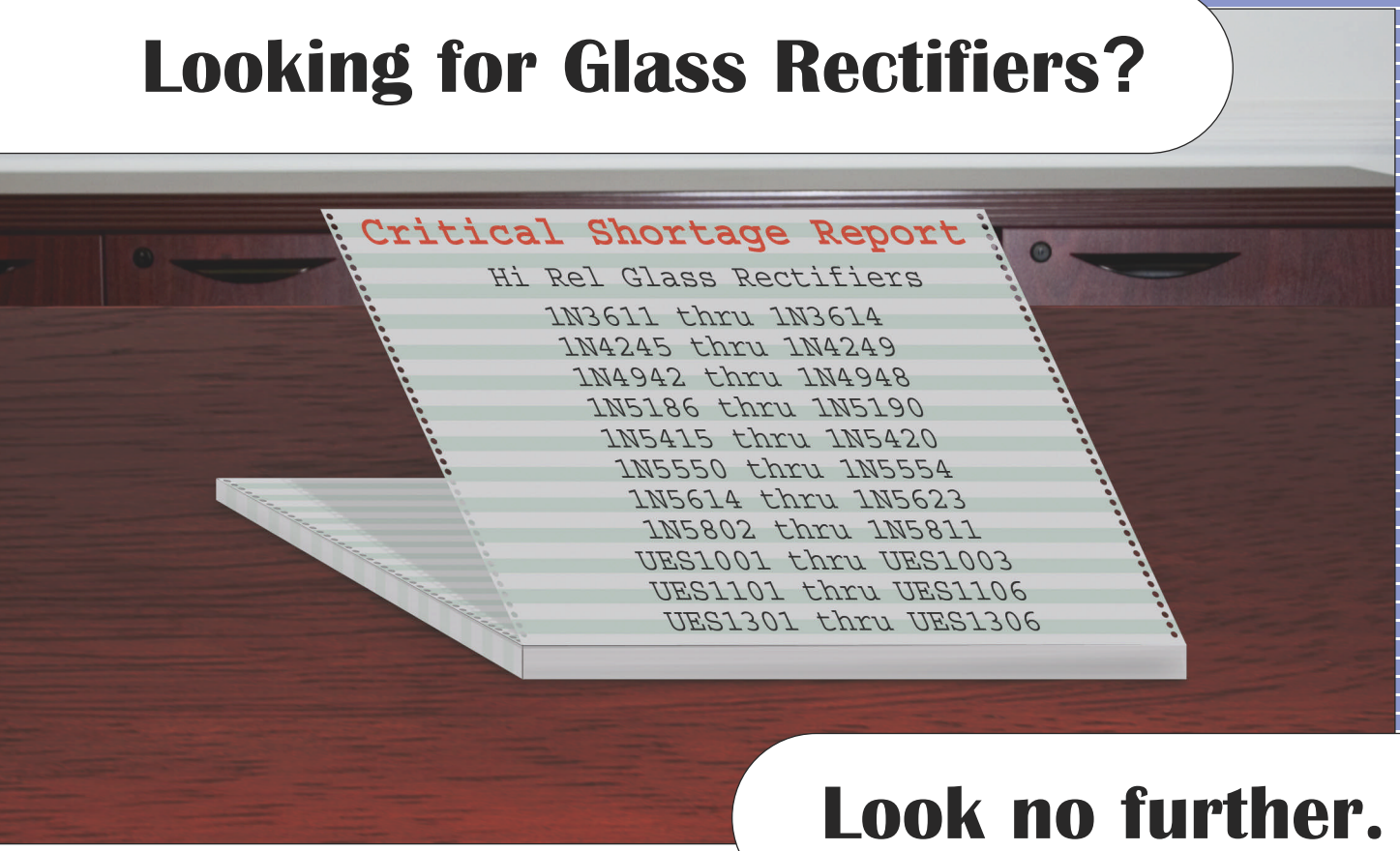

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be the best devices for your application. Even though STMicro makes controllers for both motor types, Ortmeyer suggests that you not dismiss a brushless-dc motor for your application just because PMSMs are getting all the attention now. Brushless-dc motors can use a simpler controller, and simple is always a good idea. So, how do you decide on the best motor type? Ortmeyer says that you should consider whether your application needs to use the motor for regenerative braking and whether it needs to reverse direction. For example, a washing machine needs to reverse, but it doesn't need to use the motor for braking. If you need both capabilities, you should choose a PMSM and sinusoidal control. If you need to do only reverse speed or braking, then you may well be able to get by with a brushless-dc motor and its simpler controller.

When you're determining the processing power you need, you should consider the overall system needs of your application—not just the algorithm-crunching part of motor control. Arefeen Mohammed, systems application engineer for Texas Instruments' C2000 DSC line, says that, five years ago, no one would consider using a 32-bit processor for an appliance-motor-control application, such as a washing machine. However, front-loading washing machines have a complex performance profile: The horizontal position makes them more efficiently use water but comes with a correspondingly more complex motor controller. "Now, you'll use the processor not just for motor control, but also to sense water level and temperature." He suggests you look at the overall system efficiency and not just the motor.

"Five years ago, a representative microcontroller for motor control had a 10-bit ADC with a total conversion time of about 5 µsec. Now, we offer a 12-bit ADC with a total conversion time of about 80 nsec, and we are receiving the requests to improve further. So, right now, 12 bits is a kind of standard. For advanced high-performance motor drives, we are already seeing the need for 16-bit ADCs," says Mohammed. EDN

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REFERENCE

1 Zambada, Jorge, "Sensorless Field Oriented Control of PMSM Motors," Microchip Technology, ww1.microchip.com/downloads/en/AppNotes/01078A.pdf.

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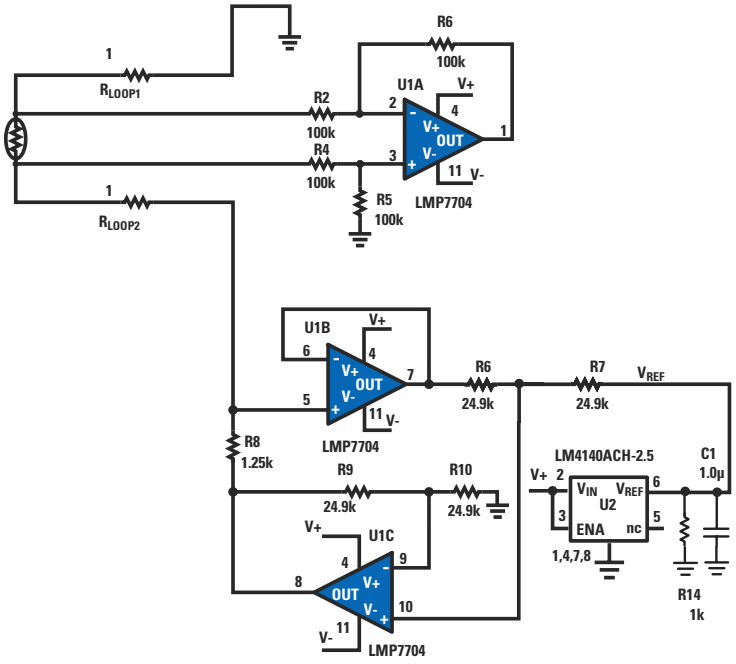

Figure 1. Typical Kelvin-Sensor Interface

This application note covers a commonly-used interface for Resistance-Temperature Detectors (RTDs) and thermistors, with improvements for common-mode rejection. When these sensors are at the end of a cable, probe leads, or even a catheter, the circuit described in this article will improve performance in the presence of common-mode noise.

RTD Standards and Specifications

Most RTDs use either platinum wire over glass or deposited on a ceramic thin-film chip. International standard EN 60751 contains RTD resistance tables, tolerances, curves, and temperature ranges.

Three common RTDs are the PT100, PT500, and PT1000, where 100, 500, and 1000 represent R_0, the 0°C resistance. From -200°C to 0°C, the resistance fits a 4th-order polynomial:

$$R = R_0(1+At+Bt^2+C(t-100)t^3)$$

From 0°C to 850°C, the resistance fits a 2nd-order polynomial:

$$R = R_0(1+At+Bt^2)$$

The coefficients are: A = 3.9083×10^{-3}/°C;
B = -5.775×10^{-7}/(°C)^2; C = -4.183×10^{-12}/(°C)^4

Recommendations

For increased sensitivity and resolution, use the highest-resistance RTD the circuit and supply voltage will allow. Low sensor current minimizes self-heating errors.

For improved common-mode rejection, the DC resistance and AC impedance from both ends of the RTD to circuit ground should be identical, with both ends of the RTD returned to the differential amplifier through a twisted-pair, doubly-shielded cable.

Choose ADC-sampling intervals consistent with the thermal time constants of the mounted sensor and object being measured. Since there will be multiple time constants, confirmation by measurement will avoid surprises.

2-, 3-, and 4-Wire Configurations

Temperature sensors can be configured in several ways: 2-wire, 3-wire, 4-wire, and 4-wire with loop. This application note covers the most common and accurate wiring configuration: the 4-wire Kelvin connection with constant-current drive. For a complete review of these configurations and corresponding recommendations, visit www.national.com, AN-1559.

Figure 1 is a typical circuit. The LM4140 is a high-precision, low-noise voltage reference. The LMP7704 is a quad, precision, CMOS RRIO op amp. U1A is a Kelvin-connected differential amplifier.

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Controlled positive feedback from U1B to U1C creates a boot-strapped (buffered Howland) current source where:

$$I_{SENSOR} = V_{REF} / R8$$

The circuit looks reasonable but has a major flaw. One end of the RTD sees ground, a low impedance, while the other end sees a current source, a high impedance. In the presence of AC fields, pickup at each end will differ and not be rejected by U1A.

In ***Figure 2,*** a 634Ω resistor (R1) and a two-pole, 30 Hz low-pass filter (U1C, R7, R8, C1, and C2) have been added to improve balance. The voltage reference and R10 are halved to keep swings within the 10 V_{DC} supply range without significantly affecting DC performance with a 5V supply and RTDs between 80Ω and 1.1k.

Above the filter passband, positive feedback from U1B to U1D is increasingly attenuated. The current source impedance drops towards 634Ω. Both ends of the RTD see similar impedances and rejection remains high until the specified open-loop gain of U1A and U1C eventually fall too low to maintain performance. A high-frequency precision op amp will improve high-frequency performance of both the current loop and the differential amplifier.

AC rejection comparisons of both circuits lend themselves very well to SPICE simulation. LMP7704 SPICE models are available at www.national.com.

For Additional Design Information

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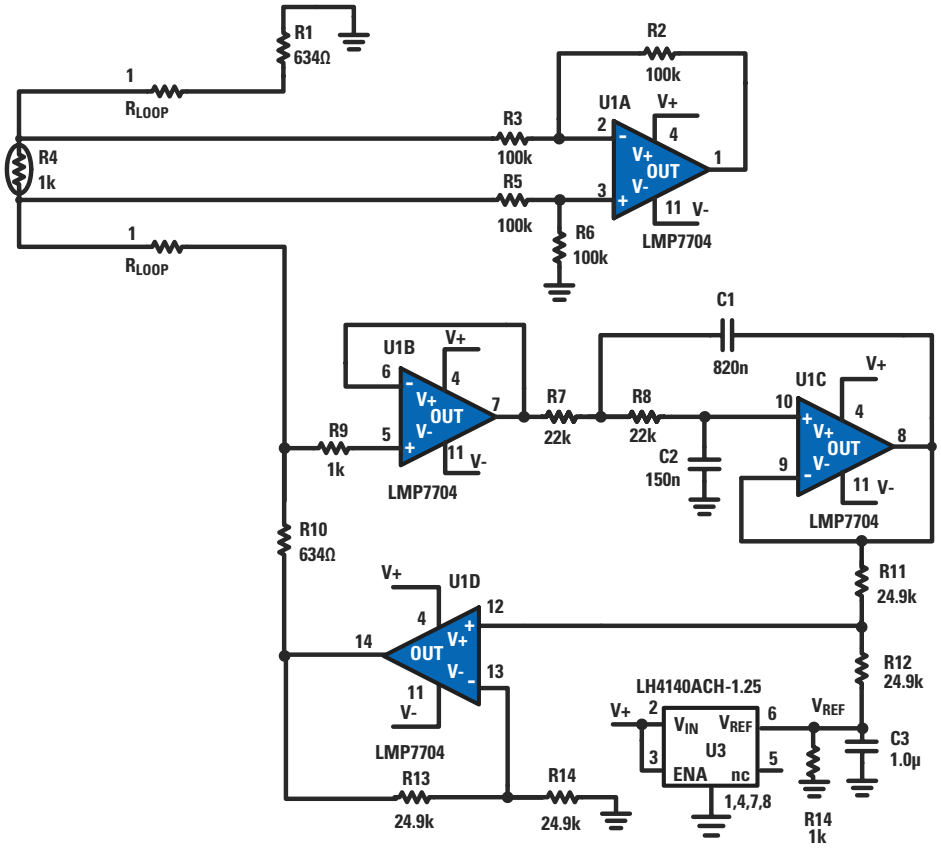

Figure 2. Improved Kelvin-Sensor Interface

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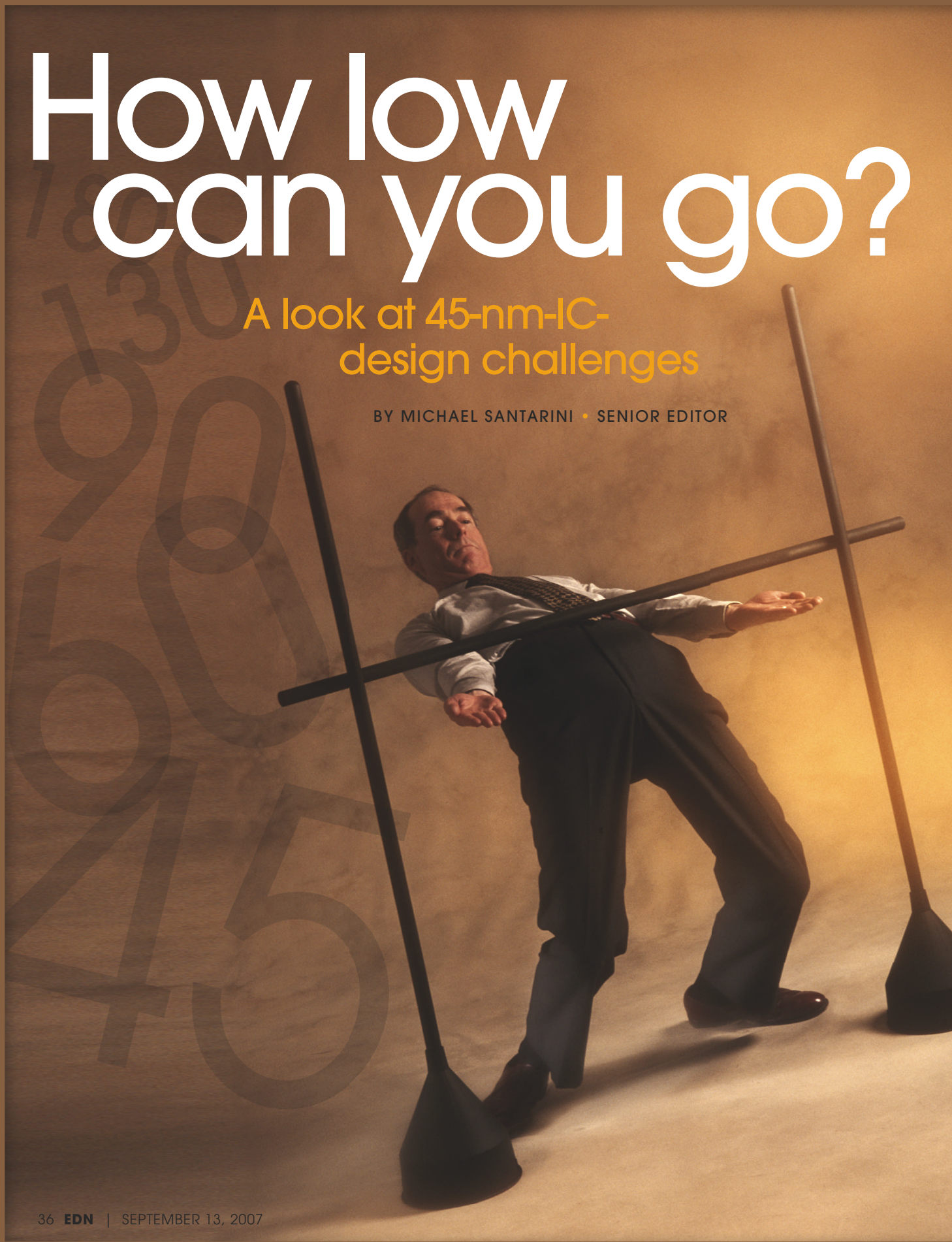
How low can you go?

A look at 45-nm-IC-design challenges

BY MICHAEL SANTARINI • SENIOR EDITOR



The 45-nm node promises SOC (system-on-chip) designers either a 40% increase in transistor counts over 65 nm or a 40% reduction in die size, but mask costs for 45-nm processes will run, at least initially, in the multimillions of dollars. Some designers—especially those with experience designing in either the 65- or the 90-nm modes and that are familiar with low-power-design techniques—will find the transition to the 45-nm process fairly straightforward. That experience may help to alleviate some of the cost burden of the transition, according to some foundries, IDMs (integrated-device manufacturers), and EDA vendors. "To design at 45 nm, you will need a better methodology, but it's not like you will need a brand-new set of tools," says Tom Quan, deputy director of design-service marketing at TSMC (Taiwan Semiconductor Manufacturing Co). "You'll just need a better methodology to use those tools."

With the introduction of 45-nm processing, foundries are now introducing RDRs (restrictive-design rules) for bulk-CMOS processes, mandating the use of advanced low-power-design techniques, and requiring the use of DFM (design-for-manufacturing) tools. Some foundries are also recommending that designers use probability-analysis tools, such as those for SSTA (statistical-static-timing analysis) and static statistical-power analysis to help reduce timing and power problems. Some hold that probability-analysis tools, although promising, may still be immature.

NO BIG CHANGES

All the big foundries say that manufacturing at the 45-nm node does not differ greatly from manufacturing at 65 nm. The two most significant changes are the 45-nm node's use of immersion lithography and its use of ultralow-k materials. Immersion, or "wet," lithography uses liquid between the projection lens and the wafer surface to enhance resolution and numerical apertures. Using the technique essentially ensures that the lithographic features of 45 nm have the same optical clarity as features at 65 nm, which means that the move to wet lithography will have little or no impact on the design flow. It will raise mask costs, however.

Top foundries TSMC; UMC (United Microelectronics Corp); and the CPTA (Common Platform Technology Alliance) of Chartered Semiconductor, IBM, and Samsung are initially introducing bulk-45-nm processes using ultralow-k-dielectric material, mainly because the processes require no vast retooling or risky process changes. But the lack of an adventurous process change also means that, as transistors shrink, so does the amount of gate oxide in those transistors; thus, leakage is worse at the 45-nm process (**Reference 1**). As a result, the large foundries working at the 45-nm node are delaying the introduction of potentially leakage-stopping materials, such as high-dielectric constant (k), into their manufacturing flows, which means that customers must do their part and, some would argue, more than their part to deal with power management.

TSMC, UMC, and the CPTA will likely have high-k materials ready for their 32-nm processes or perhaps even sooner in second-generation, high-performance, 45-nm processes. Foundries have become wary of any material changes in their processes after experiencing severe setbacks when they introduced 130-nm processes that employed both low-k and copper materials. First, designs at that node had tremendous yield problems and failure rates and essentially drove a retooling in the EDA industry to timing-closure-tool flows, which proved good for EDA vendors but bad for users and chip manufacturers. "As you might expect, foundries are also holding their high-k developments close to the vest because they believe they can use them

IF YOU HAVE TOOLS FOR THE 65-NM OR EVEN THE 90-NM NODE, MOVING TO THE 45-NM NODE REQUIRES NO RETOOLING. BUT DESIGNERS MOVING TO THIS NODE MUST ADOPT SOME ADVANCED DESIGN TECHNIQUES AND BE AWARE OF SOME NEW DESIGN RULES THAT FOUNDRIES HAVE IMPOSED TO ENSURE THAT SOC DESIGNS YIELD ACCEPTABLE RESULTS.

as competitive advantages," says Walter Ng, senior director for design solutions at Chartered Semiconductor.

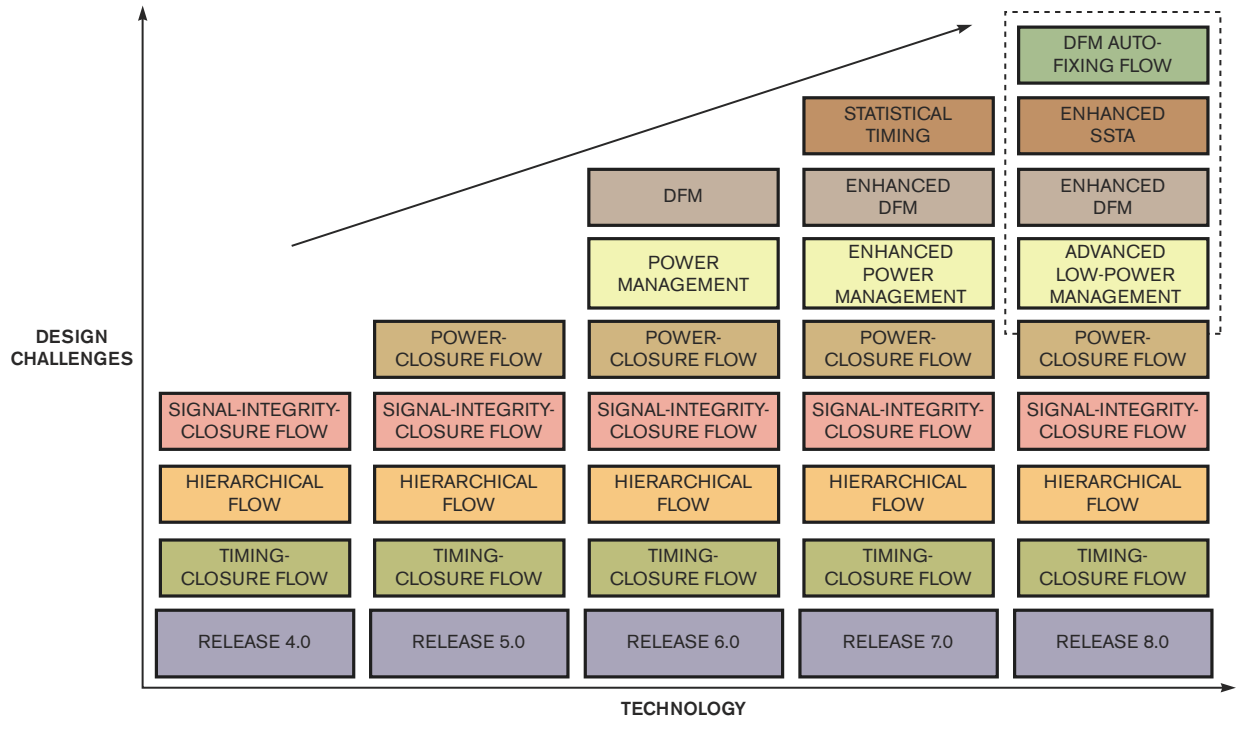
In the meantime, however, foundries TSMC, UMC, and the CPTA plan to have 45-nm processes with ultralow-k in pilot or even mass production by year's end and say that they have been working with the major EDA vendors over the past 18 months to ensure that the vendors' tools can handle leakage and other design challenges. Foundries and EDA vendors have high hopes for the 45-nm node. For example, EDA vendor Synopsys had 17 customers doing 65 45-nm designs, and five customers had 10 45-nm tapeouts, according to John Chilton, the company's senior vice president of marketing and strategic development. "It is spookily like 65-nm design two years ago," he says. "Those numbers were the same, and they tracked quarter after quarter. Right now, there are 425 active 65-nm designs and about 190 tapeouts. So, that tells you that, in the next two years, we'll see about another 180 tapeouts at 45 nm, so things will be pretty active." Some foundries hope that the 45-nm process will become even more active than the 65-nm process and that most chip designers now doing 130-nm design will be tempted to skip the 90- and 65-nm nodes and jump right into the 45-nm process, noting that these incremental, rather than abrupt, changes in manufacturing mean that the design flow should also change incrementally.

AT A GLANCE

- The 45-nm node offers a 40% reduction in die size or a 40% increase in gate counts over the 65-nm node.
- Active and standby leakage accounts for 60 to 65% of a 45-nm IC's overall power consumption.
- Low-power techniques are necessary at the 45-nm node.
- DFM (design-for-manufacturing) tools are musts at the 45-nm node.
- Foundries are starting to use RDRs (restrictive-design rules) for bulk-CMOS processes at 45 nm.
- Maturing probability-analysis tools will be "nice-to-have" features rather than "must haves" for the 45-nm process.

CHALLENGES AT 45 NM

Foundries, design teams, and EDA companies say that the 45-nm process presents three major challenges for design teams: mandatory low-power design, mandatory use of DFM tools and methods, and increased deployment of RDRs and probability analysis. As was the case at the 65-nm node, the foundries' first process lines for the 45-nm node are for low power, rather than high performance. Rather than bite the bullet and employ new materials, such as high-k, foundries are not making drastic changes. This decision means that leakage continues to be a first-order concern at the 45-nm node. At the 65-nm node, dynamic and static, or standby, leakage accounts for 40% of an IC's overall power consumption and forces all SOC designers, regardless of their targeted end application, to employ low-power-de-



TSMC has issued reference flows for the last five generations of products. Each successive generation has called for more tools illustrating the rising complexity in design requirements.

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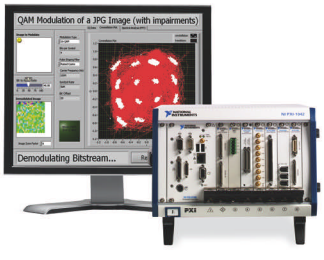

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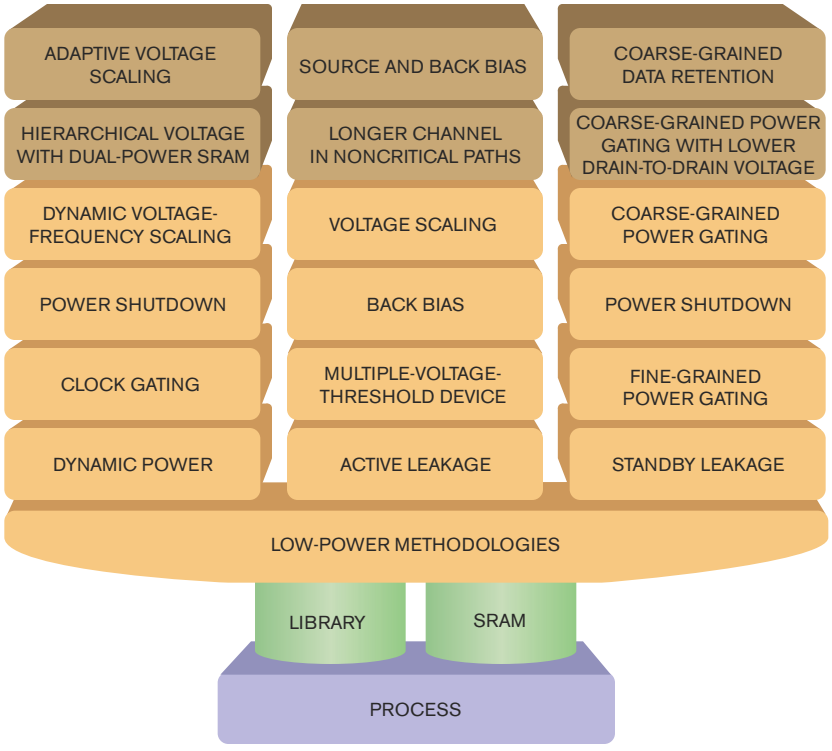
sign techniques (**Reference 2**). At the 45-nm node, the problem becomes immense: Leakage consumes 60 to 65% of a device's overall power. This leakage necessitates the use of low-power-design techniques, according to foundries. "We're seeing a lot more use of voltage islands, for example," says Chartered Semiconductor's Ng. "And customers aren't employing voltage islands to simply group devices by power-supply requirements; they are using them to shut down entire sections of devices when they are not in use. Those are drastic techniques for power management, and we're seeing a lot more of that."

Gregg Bartlett, vice president of CMOS technology at Freescale, says that Freescale's networking and wireless groups are designing at the 45-nm node, and both are employing low-power techniques. "I would describe the transition from 65 to 45 nm as nonrevolutionary," says Bartlett. "In power-management-design techniques, we have been doing dynamic-voltage-frequency scaling, gate-retention power gating, and other power-saving techniques for a few nodes. They are not new to us at 45 nm, but we are applying more of them." Bartlett notes that Freescale's wireless group, which has specialized in low-power design for several process nodes, is spending more time doing sophisticated power modeling and is also starting to use thermal modeling for its 45-nm tool flow.

"Locating hot spots and points of intradie thermal variations and knowing where your points of power dissipation are the strongest are areas we see as emerging requirements," says Bartlett. "Although these techniques and tools are not mainstream yet, they give you the comfort of better understanding the product space your products are going to go into." He notes that Freescale has been using IBM's SOI (silicon-on-insulator) processes for its last few generations of chip sets. "We're constantly evaluating processes, but we've had great results with SOI," he says. "We've seen a double-digit improvement in both power and performance in SOI over bulk-CMOS processes."

But foundries offering bulk CMOS have been doing a lot of work to manage power in their new ultralow-k processes, and they've also been working closely with EDA vendors to give customers more tools to help them manage power with the 45-nm process. For example, in its 8.0 reference flow, TSMC has added "enhanced low-power-technique recommendations" to help customers achieve further power savings. The foundry recommends the use of advanced voltage scaling and hierarchical voltage with dual-power SRAM blocks to deal with dynamic-power management, the use of source- and back-biasing, and the use of longer channels in noncritical paths to reduce active leakage. It also recommends the use of coarse-grained data retention and power gating with lower drain-to-drain voltage to minimize standby-power leakage.



Power management remains a top priority for 45-nm design. TSMC has added more power-management features to an already-long list of power-management techniques.

> "THESE TECHNIQUES AND TOOLS ... GIVE YOU THE COMFORT OF BETTER UNDERSTANDING THE PRODUCT SPACE YOUR PRODUCTS ARE GOING TO GO INTO."

"Most of these techniques are about gating a clock or simply shutting down blocks when you are not using them," says TSMC's Quan. "There are a multitude of techniques here that our customers can now employ when they start designing in the 45-nm node." There is also a multitude of low-power commercial tools now available to customers. TSMC, UMC, and the CPTA have qualified all of the large vendors' power and low-power point tools from privately held companies. Cadence, Synopsys, and Magma all field low-power tools, and each is diligently working to create an all-in-one low-power flow to capture seats as designers target IC designs to run on leakage-prone 65- and 45-nm processes.

Foundries are eager to accommodate EDA companies in this task. For its 8.0 reference flow, TSMC has validated the Cadence-backed CPF (Common Power Format), which is under the auspices of the Si2 (Silicon Integration

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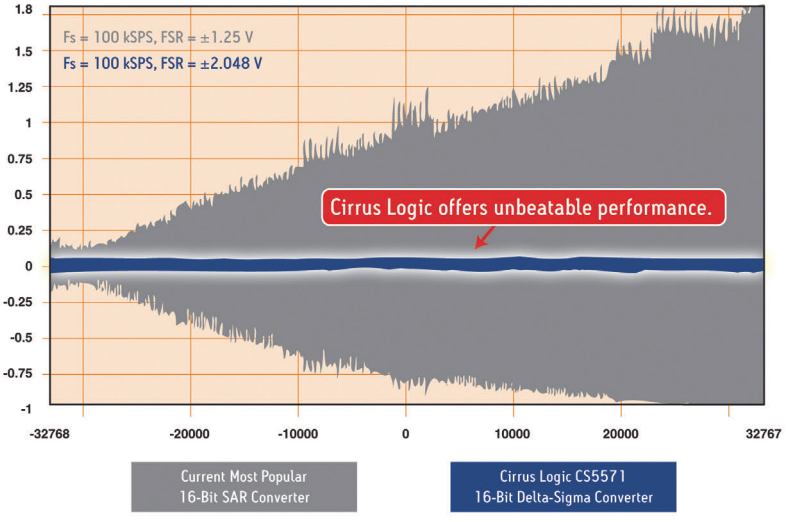

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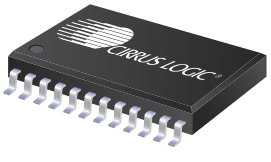
CS5580	16 bits	200 kSPS	0.1LSB	1, Differential	70 mW
CS5581	16 bits	200 kSPS	0.1LSB	1, Single-ended	70 mW



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Initiative). The format promises to allow tools from across the design flow to work from a single power format. Quan notes that TSMC is also working with Accellera's UPF (Unified Power Format) group to validate the format for its 45-nm process.

DFM BECOMES A MUST

At the 65-nm node, foundries were recommending but not requiring their customers' use of DFM tools (**Reference 3**). However, the 45-nm node will require the use of DFM tools for two of three categories the foundries have defined: LPC (lithography-process checking) and CAA (critical-area analysis). However, foundries will recommend but not require the use of DFM tools for a third category, CMP (chemical-mechanical-planarization) simulation. "We haven't seen many customers using DFM tools at the 65-nm node," says Chartered's Ng. "I'd be surprised if any customer tries to tackle 45 nm without using some amount of DFM." He notes that foundries used the 65-nm process as a proving ground for DFM tools. "We were just starting to become familiar with DFM issues and tool requirements," says Ng. "Now, at the 45-nm node, we have a better idea of what is truly needed."

Most large EDA companies now have the required DFM tools and are trying to integrate them into technologies. Over the last year, most filled out their tool lineups either through internal development or through mergers with and acquisitions of DFM companies. In many cases, the vendors are diligently integrating DFM technologies into tools so that users won't even know they are employing these tools. The major foundries have been helping the EDA companies in this endeavor and have taken note that EDA vendors are now integrating DFM technologies into their flows and making implementation tools correct by construction or at least DFM-compliant. This scenario is similiar to the way routers became DRC (design-rules-checking)-compliant during the era of the 90- and 130-nm processes.

Correct-by-construction DFM, or "in-the-loop-design verification," as Magma Design Automation calls it, is somewhat of a necessity, says Dwayne Burek, senior

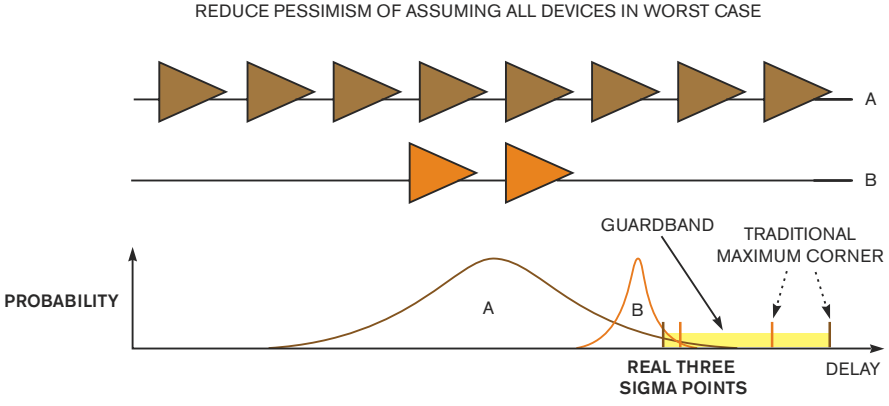
MOST LARGE EDA COMPANIES NOW HAVE THE REQUIRED DFM TOOLS AND ARE TRYING TO INTEGRATE THEM INTO TECHNOLOGIES.

product director of the company's design-implementation-business unit. The 45 nm-node's massive layouts require a great number of DFM decks and models on top of the ever-growing number of DRC/LVS (layout-versus-schematic) physical-verification decks and models. Burek notes that Magma's Talus platform has an in-the-loop-design-verification capability, which includes DRC, LPC, and CMP simulation. "You can run checks within the implementation flow natively or with an integrated physical-verification capability," says Burek.

Both Magma's and Cadence's tool flows have built-in LPC, CMP simulation, and CAA. Cadence recently announced the addition of Aura lithography technology and space-based routing to its Encounter tools and gained LPC and CAA tools from its August acquisition of Clear Shape Technologies. Synopsys' and Mentor Graphics' flows also incorporate LPC and CAA tools, but the two companies use CMP simulators from foundries. TSMC and UMC traditionally work with all EDA vendors interested in validating their tools on the foundries' new processes. TSMC has validated all the large tool vendors' flows and many privately held companies' DFM tools, because this validation makes TSMC's fabrication data available to partner companies in an encrypted format. Quan says that making this data available eases tool vendors' ability to offer the company's customers what TSMC calls DFM-autofixing flows.

UMC also creates a reference flow for every design, but Mort Bamdad, senior director of the corporate marketing division at the company, says UMC doesn't dictate how designs must be done. "As far as 45 nm goes, the baseline flow doesn't change much," he says. "We are talking to EDA vendors to implement DFM changes in their tools so designers will not need new tools but may need some new features."

As with the 65-nm node, the CPTA hand-picked DFM-vendor tools for its 45-nm DFM flow. For CAA, the CPTA has qualified tools from Ponte Solutions and Mentor Graphics. For CMP simulation, the company has qualified Cadence's CMP Predictor, which it obtained when it acquired Praesagus. For detailed, block-level LPC/simulation, the CPTA has qualified Mentor's LFD (lithography-friendly-design) tool, and, for chip-level LPC, the CPTA has qualified Cadence/Clear Shape's InShape tools. Ng notes that the CPTA also recommends Blaze DFM's MO to reduce leakage and improve yield and recom-



SSTA holds promise in improving performance and lowering power. The technology is maturing, but it remains to be seen whether the 45-nm node will broadly adopt it.

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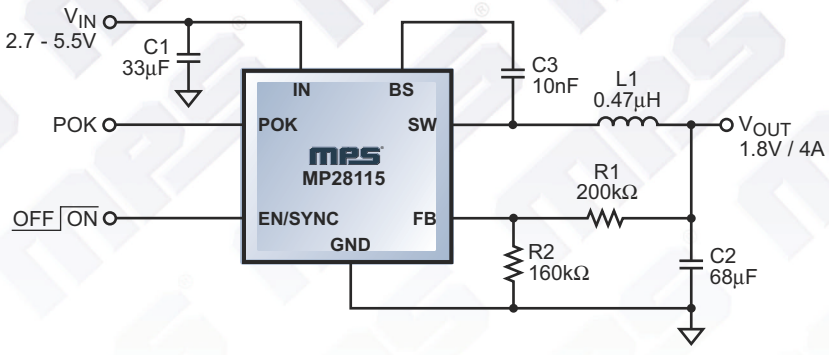

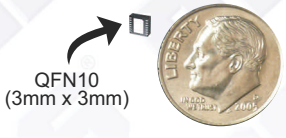

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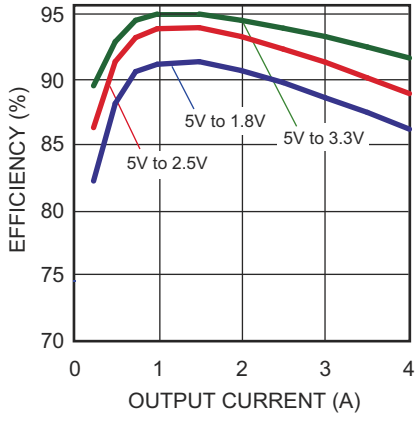

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RDRs: NICE TO HAVE?

Over the last few years, industry luminaries have been warning that, with the increase in design size, number of design-rule files, number of DFM issues—especially lithography—and increase in mask costs, foundries would soon need to start enforcing more RDRs to help design teams produce good IC yields. At the 45-nm node, some foundries are seriously considering enforcing these rules. For example, UMC has for two years been developing its 45-nm process. It debuted its first 45-nm test vehicle in the first quarter of 2006 and expects to have introduced its first five early tapeouts by the third quarter of this year and have its 45-nm LL (low-leakage) process ready for pilot production by year-end. UMC's Bamdad says that, in ironing out the process, the company has seen great promise for the use of RDRs to help customers quickly get high-yielding designs to market. "For example, the orientation of polysilicon is becoming one of the big issues," says Bamdad. "We're still working on all the details, but it might become mandatory that customers lay polysilicon in the same direction they are laying SRAM and standard cells … horizontally rather than vertically. Also, if you are going to have an L shape in your design, you'll have to change layers—go horizontally [with the] via and contact and then go vertically. These are rules we expect to enforce."

MORE AT EDN.COM

- For more on SSTA (statistical-static-timing analysis), see "Characterization tool aids SSTA-library creation" at www.edn.com/article/CA6407294.
- For another perspective on 90-nm-chip design, see Executive Editor Ron Wilson's article "Is chip design different after 90 nm?" at www.edn.com/article/CA6347251.
- Go to www.edn.com/070913cs and click on Feedback Loop to post a comment on this article.

Chartered's Ng says that, although the company's process-alliance partner IBM has enforced RDRs for its SOI process, the CPTA's customers are now requesting these rules for the CPTA's bulk-CMOS offerings. Many hope that the proper use of RDRs could increase the chance that design teams will be able to create "right-the-first-time" designs and not incur heavy re-spin or ever-more-painful extra mask costs.

Joe Sawicki, vice president and general manager of Mentor's design-to-silicon division, says that, because immersion lithography produces essentially the same quality of results as dry lithography for the 65-nm node, the 45-nm node may not yet require RDRs. "If you were doing without RDRs at 65 nm, you can probably do without them at 45 nm," he says. "The entire impetus behind RDRs is that 2-D features are [difficult to implement]. If you just look at the mathematics, what's going to happen when you go from 45 nm to 32 nm and 22 nm is that features inevitably go from being [difficult to implement] to your having no idea how to make them happen.

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When you hit 22 nm, if you believe that you can do [those 2-D features] with a single etch or a single mask process, [you will] have to change the laws of physics." RDRs are ways to help foundries introduce processes at new nodes without radically changing the manufacturing equipment and flows, he says. He notes, however, that some other advances in lithography and manufacturing may make RDRs less necessary at the 32- and 22-nm nodes.

Synopsys' Chilton says that his company has yet to hear of any customers using RDRs. "So far, people seem to be sticking to classic design rules, though it's moving to model-based rather than rules-based approaches," he says. RDRs are somewhat controversial and have spurred a debate in the industry about whether they will help alleviate some of the complexity in design flows or will overtax commercial routers that must deal with massive DFM rules and models on top of ever-increasing DRC decks for ever-larger-gate-count designs.

Foundry reps indicate that, in qualifying implementation flows even without RDRs, some commercial routers—but they decline to say which ones—that worked for the 65-nm node struggle with the large designs and more complex rules and models at 45 nm. Fortunately, EDA vendors are addressing these problems. Mentor and Cadence both claim to have new router technology that they created to handle the complexities of 45 nm. Mentor Graphics acquired Sierra Design Automation in June and is currently working with foundries to qualify its router for 45-nm flows and further integrate its Calibre lineup into the flow, and Cadence this month added technology from its custom digital-space-based-router technology to its standard-cell Encounter routing platform. "The 65- and especially the 45-nm nodes are separating the great routers from the OK routers," says Eric Filseth, vice president of digital-IC implementation at Cadence.

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PROBABILITY ANALYSIS

Although the academic and EDA communities have predicted that probability-analysis tools—notably SSTA (statistical-static-timing-analysis)tools—would replace traditional static-analysis tools at advanced nodes, that scenario hasn't occurred at the 65-nm node, according to foundries. But EDA vendors,

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early adopters of 45-nm technology, and foundry reps from TSMC and UMC say that 45 nm may mark the first node to broadly adopt probability analysis. SSTA tools promise to replace worst-case-timing models (traditional wire-load models) with more realistic and accurate analysis of circuit behavior using statistical techniques. Using statistical models to characterize standard-cell-process libraries, designers run analysis of the behavior of circuits, blocks, or entire designs and derive timing parameters of circuit performance. They then use those results to fine-tune the performance of their designs and even reduce power or toggle off unneeded transistors or blocks.

With the increasing size and complexity of 45-nm designs, SSTA tools have proved useful for some designers, including those at Texas Instruments, according to Mike Fazeli, the company's worldwide-EDA-strategy manager, and Clive Bittlestone, TI's ASIC-backplane manager. Despite the tools' usefulness, however, foundries have been slow to approve them for timing sign-off, slowing their adoption. Other designers have found commercial SSTA difficult to use. "Variation is tricky because it calls into question things in sign-off and where you should set the variation points," says Synopsys' Chilton. "It is hard to figure out. So, it's a big move from traditional rules-based sign-off to something softer; there's a culture to figure out—not a technical problem."

Chartered Semiconductor's Ng is skeptical about whether SSTA tools will be in wide use at the 45-nm node. "It's an area that everyone agrees has a lot of promise; the problem is in implementation," he says. However, EDA companies and some foundries, including TSMC and UMC, say that the predictability-analysis tools are maturing. EDA companies, such as Extreme DA, Magma, and Synopsys, have been fielding SSTA tools for more than a year, and Cadence also jumped into the game this month with its Encounter Timing System GXL SSTA tool. TSMC's Quan says that SSTA standard-cell-library-characterization tools, such as Altos Design Automation's Variety, have helped solidify the flow because the tools can help foundries and users characterize libraries for better use of statistical-analysis tools. TSMC has added Altos Design to its 8.0 reference flow and is now offering customers statistical models of its 45-nm process. Designers can extend TSMC's statistical models and methods to leakage issues, and TSMC has added statistical leakage analysis to its 8.0 reference flow, although EDA vendors, such as Magma, are just starting to offer these types of tools.

MORE CHALLENGES

Overall, foundries expect the transition to the 45-nm node to be fairly easy for designers familiar with the challenges of 65-nm and even 90-nm design. The node will require designers to implement low-power-design techniques and to use DFM tools and may require the use of RDRs and probability-analysis tools, too. Foundries hope that the 45-nm node will prove so unthreatening to mainstream-IC designers that a large chunk of them working at the 130-nm node will consider skipping right over 90 and 65 nm and go straight into 45 nm. But, before you face the 45-nm test, you should also consider the ongoing challenges inherent in every new design process: The 45-nm node will present significant challenges in developing chip architectures, software development, logic design, and logic verification. EDN

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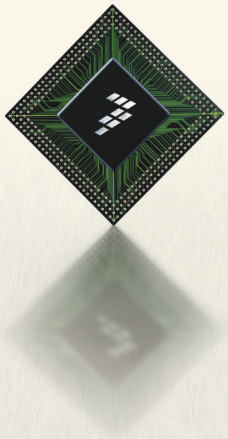

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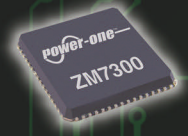

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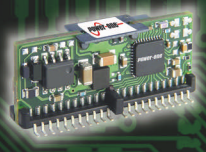

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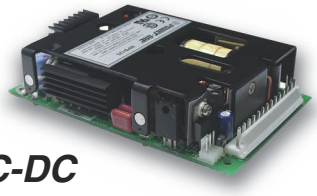

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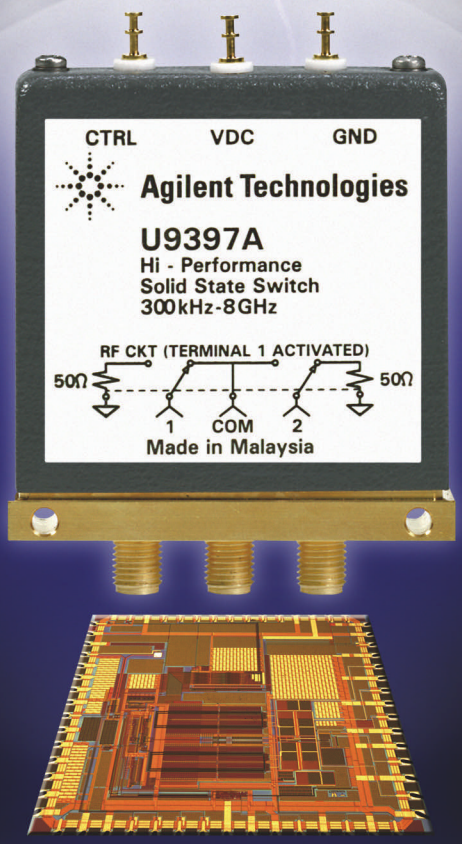

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Distributed linear regulators increase output current and spread the heat

PARALLEL-BOARD LAYOUT AND HEAT SPREADING PROVIDE DESIGNERS NEW WAYS TO USE LINEAR REGULATORS IN ALL-SURFACE-MOUNT APPROACHES. THESE TECHNIQUES WORK WELL IN TODAY'S HIGH-PERFORMANCE, HIGH-DENSITY PCBs.

Modern system boards include big, current-hungry digital ICs along with a plethora of other lower-current digital and analog circuitry. Such a system board can require as many as five or six power supplies, depending on the number and types of ICs you use. Moreover, some circuits, such as audio or high-speed serial links, are noise-sensitive and generally require designers to use inherently quieter linear regulators. Heat problems accompany the use of multiple power supplies; therefore, designers must add heat sinks along with various types of regulators. But the heat sinks make the board more cumbersome and harder to assemble than an all-surface-mount approach. A sly designer can turn to techniques such as using parallel regulators and using the PCB (printed-circuit board) itself for cooling to develop an all-surface-mount design.

When you employ surface-mounted regulators, thermal conduction and air cooling limit the amount of power that each chip can internally dissipate. With a typical board, allowing a maximum ambient temperature of 60 to 70°C, a surface-mounted linear regulator can dissipate approximately 1 to 2W. The total dissipation depends on the heat spreading of the board and the airflow across the board. If a design must dissipate more power, the engineer generally mounts the regulator on a heat sink to achieve the higher power levels with no thermal problems. Paralleling regulators on the board spreads

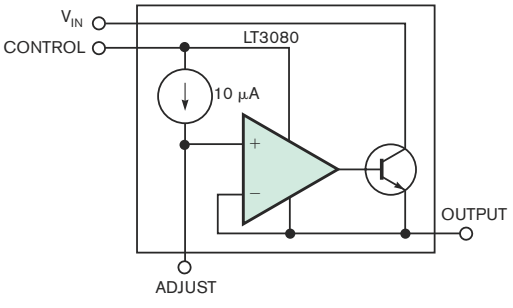

Figure 1 This parallel-capable regulator uses a 10-µA current source as a reference. The internal op amp keeps the adjustment and output terminals within a few millivolts.

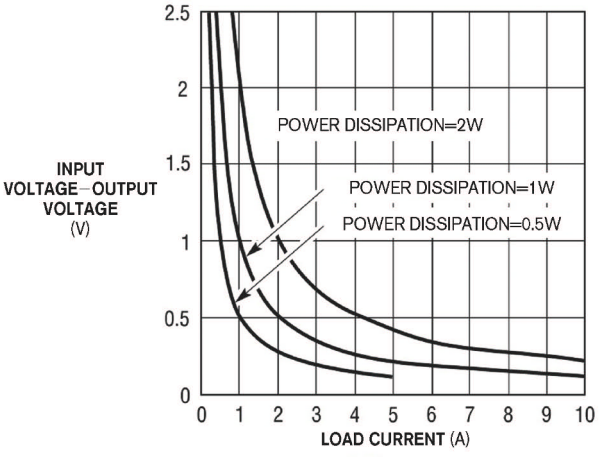

Figure 2 The available output current as a function of I/O differential and power dissipation allows 2W maximum power dissipation; thus, a design can deliver 1A output currents even with 1 to 2V I/O differential.

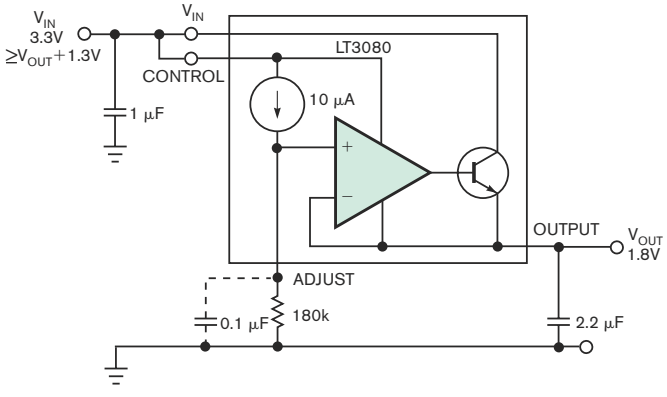

Figure 3 This basic configuration yields a 1.8V output. The design ties together the input and the control pins, and a resistor sets the output voltage. A 2.2-µF output capacitor ensures stability. If you adjust the adjustment resistor to zero, the output is zero.

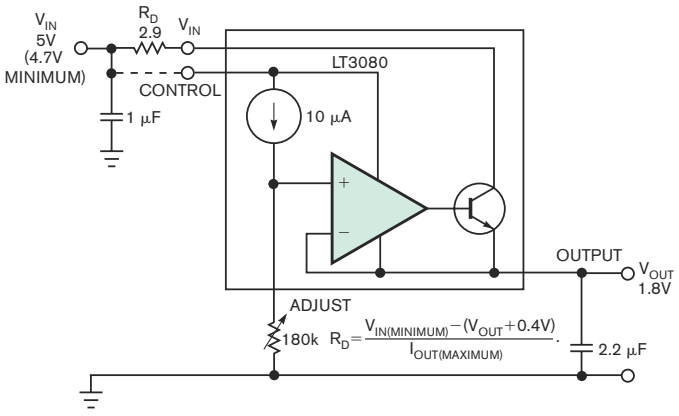

Figure 4 To spread power, a designer can add a resistor in series with the power pin of the device. Such a circuit separates part of the power dissipation from the regulator. This technique spreads the power dissipation around the surface-mount board rather than concentrating all of the power dissipation in the regulator.

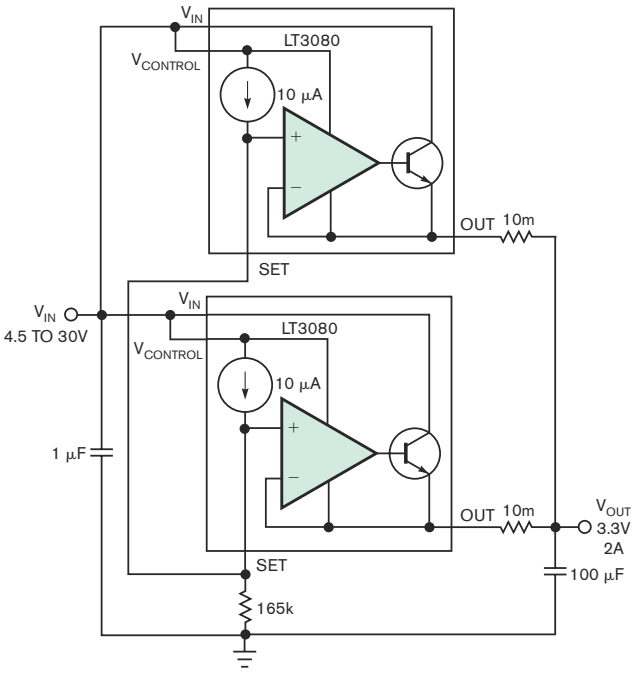

Figure 5 Placing regulators in parallel spreads heat for a surface-mount design. The schematic shows two regulators in parallel to deliver higher output current. You can add even more regulators in parallel for even higher output currents. The design in this instance ensures current sharing by using a 10-mΩ PCB trace that acts as a ballast resistor.

the heat, provides greater maximum output current than does a single-regulator design, and helps maintain low peak temperatures.

Figure 1 shows a parallel-capable adjustable regulator. A precision 0 TC (temperature coefficient)—less than 1% over temperature—of 10-µA internal-current source connects to

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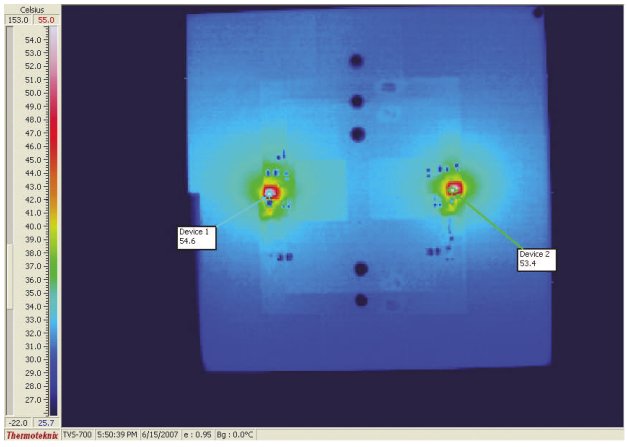

Figure 6 With a differential of 0.7V, dissipation is 0.7W, and temperature rises 28°C on a two-sided PCB.

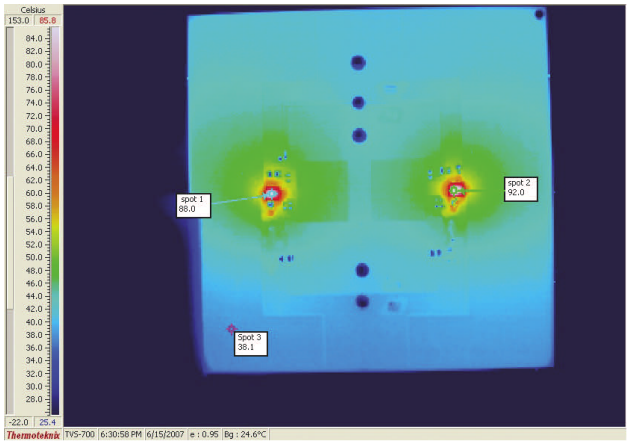

Figure 7 With a differential of 1.7V, dissipation is 1.7W, and temperature rises 65°C on a two-sided PCB.

the noninverting input of a power operational amplifier. The amplifier provides a low-impedance, buffered output, which the voltage on the noninverting input controls. The control and input pins connect, input and output capacitors add stability, and a resistor from the adjust pin sets the output voltage. A 180-kΩ resistor from the noninverting input to ground provides the 1.8V output. A short or a 0Ω resistor would set the output to 0V. Designers can control the output with a resistor or with a DAC, adjusting the output from 0V to the maximum that the input power supply defines. The design requires a minimum load current of 1 mA because it has no ground pin. An optional 0.1-µF capacitor reduces noise.

HOW MUCH POWER?

In considering such a power source, a designer would need to determine how much power the circuit can deliver relative to the heat dissipated. As a rule of thumb for temperature rise on PCBs, you can expect approximately 40°C/1W rise. With

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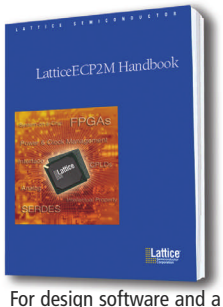

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a 60°C ambient temperature, 1W would raise the temperature to 100°C. The temperature rise at 2W puts the 140°C peak temperature above the safe operating temperature on most semiconductors. The designer would need either a high-thermal-conductivity board or airflow to keep the peak temperature down. A designer can implement a 1.1A supply regulating from 2.5 to 1.8V or 1.8 to 1.2V directly on a PCB. For the same peak operating temperatures, the power dissipation can limit the output current for 5 to 3.3V or 3.3 to 1.5V, depending on ambient temperature and airflow.

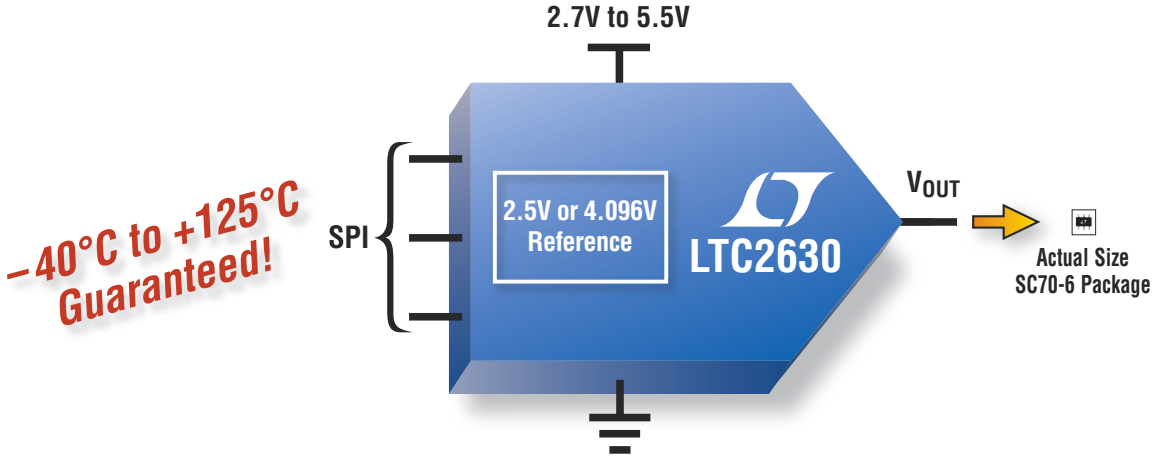
Figure 2 shows the maximum output current at different I/O differentials for a regulator when the power dissipation is 1 or 2W. To remain generally useful in many circuits, a regulator must support 2W. Paralleling regulators or using circuit tricks to spread the heat allows higher power dissipation and higher output currents. You can spread the power dissipation among several devices so that no hot spots result in the system board. If your application requires more current than a single regulator can supply, you can add a second regulator.

Designers can also use other tricks to dissipate the heat. For instance, you can move some of the power dissipation—that is, heat—from the regulator to an external resistor, thereby reducing the peak temperature of the regulator. Instead of having one point with a 80°C rise, you can spread the heat to two points, each with a 40°C rise. You can place the resistor directly in series with the regulator as long as the input voltage at the regulator at maximum current does not place the regulator into dropout. This technique is most useful in multiple-output power systems in which the input is regulated and the regulator is generating an additional voltage. Some regulator designs separately expose the power and the control circuitry. In such cases, the dropout on the power pin is only 100 to 300 mV, allowing connection to a lower voltage supply to reduce dissipation. If you use the resistor only in series with the power input, the design can transfer more power to the resistor without dropout.

Figure 3 shows the collector of the output transistor connected to split the power dissipation between the internal power transistor and an external resistor. In this example, a designer can place a maximum resistor of 2.9Ω in series with the input, and the regulator won't enter a dropout state. At full load, the design drops approximately 2.9V across the external resistor, and the external resistor dissipates about 3W. To minimize peak temperatures on a PCB, you can break this resistance value into several 1Ω resistors across the board. The power dissipation in the regulator peaks at approximately 750 mW when the power dissipation in the resistors and the power dissipation in the transistor are equal. The copper planes in the PCB easily handle this power. In actual systems, you should ensure that less than 2.9V drops across the resistor to allow for tolerance in the 5V input supply.

If you need higher output current, consider using regulators in parallel to share the power demand. In such a design, you should tie together the adjust, output, and input pins. You should connect the input pins when you use an external series resistor or connect directly to an input-voltage supply. Although you should connect the outputs, you must also ensure current sharing using a ballast on each output. The size of

SC70 12-Bit DAC with Internal Reference



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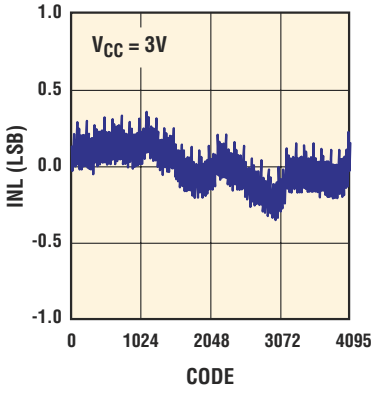

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the ballast depends on the voltage mismatch between the regulators. The ballast must drop enough voltage to absorb the output difference. Without the ballast, one regulator supplies all the current until it reaches its limit before the next regulator turns on—an unreliable situation.

In regulators that use op amps as the output-power stage, the offset voltage determines the mismatch between regulators, which is in the millivolt range. This situation requires 10- to 20-mΩ ballast resistors. But you need not add actual resistors. Instead, you can rely on a small piece of PCB trace. A ballast drop of only 10 mV still allows good regulation—1% at 1V output. For this level of ballast, you must ensure that regulator-dc errors are less than the ballast drop. For a 1-oz board, a 10-mΩ ballast requires a trace width of 180 at 10 mil and 370 at 20 mil. For a 2-oz board, the corresponding figures are 370 and 470.

Figure 4 shows a design that uses parallel regulators. The two devices have a 10-mΩ ballast resistor. At full output current, this design gives better than 80% equalized sharing of the current. The external resistance of 10 mΩ (5 mΩ for the two devices in parallel) adds only approximately 10 mV of output-regulation drop at an output of 2A. With a 3.3V output, this drop adds only 0.3% error to the regulation. You can use more than two regulators in parallel for even higher output current. Spread the regulators on the PCB to spread the heat. You can also use input resistors to further spread the heat if the I/O difference is high.

THERMAL PERFORMANCE

Consider the thermal performance of a parallel-regulator design. For example, assume QFN devices mounted on a double-sided PCB. The design locates the regulators approximately 1.5 in. apart. Also assume that you will vertically mount the board for convection cooling. Two tests on such a board measure the peak temperature and current sharing of these devices. In the first test, the circuit operates with an approximately 0.7V input-to-output differential, and each regulator produces 1A. This configuration produces 700-mW dissipation in each device and a cumulative 2A output current. The test yielded a temperature rise above ambient of approximately 28°C, and both devices were within ±1°C. The test demonstrated excellent thermal- and electrical-sharing characteristics. **Figure 5** shows the temperature distribution between the regulators and the PCB, and the peak temperature reaches ambient temperature within approximately 0.5 in. of the devices.

The test then increased the power demand with a 1.7V differential across each device. This second test resulted in 1.7W dissipation in each device and a device temperature of approximately 90°C—about 65°C above ambient temperature (**figures 6** and **7**). The test revealed that temperature matching between the regulators is within 2°. The board temperature decreased to approximately 40°C within approximately 0.75 in. of each device. Although 95°C is an acceptable operating temperature for the tested regulators, the rise in these tests was in a 25°C ambient environment. For higher ambient temperatures, designers must control the temperature to prevent device temperatures from exceeding 125°C. A 3m/sec airflow across the devices decreases the device temperature by approximately 20°C, providing margin for higher operating ambient temperatures. In addition, this test relied on a two-layer board. A four-layer board would provide better power dissipation.

Parallel-board layout and heat spreading provide designers new ways to use linear regulators in all-surface-mount approaches. These techniques work well in today's high-performance, high-density PCBs. To achieve good sharing performance, your design must carefully control the dc characteristics in the regulator. Once designers understand the control characteristics, they can routinely parallel regulators and spread heat to achieve all-surface-mount systems. EDN

AUTHOR'S BIOGRAPHY

Robert Dobkin is a founder and chief technical officer of Linear Technology Corp. Before founding Linear Technology in 1981, Dobkin was director of advanced circuit development at National Semiconductor. His personal interests include sports and antique cars, flying, music, and investing.

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DESIGN NOTES

Buck-Boost Controller Simplifies Design of DC/DC Converters for Handheld Products – Design Note 424

David Burgoon

Introduction

A number of conventional solutions have been available for the design of a DC/DC converter where the output voltage is within the input voltage range—a common scenario in Li-Ion battery-powered applications—but none were very attractive until now. Conventional topologies, such as SEPIC or boost followed by buck, have numerous disadvantages, including low efficiency, complex magnetics, polarity inversion and/or circuit complexity/cost. The LTC®3785 buck-boost controller yields a simple, efficient, low parts-count, single-converter solution that is easy to implement, thus avoiding the drawbacks associated with traditional solutions.

High Efficiency Controller Capabilities

The LTC3785 serves applications requiring input and output voltages in the range of 2.7 to 10V—ideal for applications powered from one or two Li-Ion cells or multiple cell NiMH, NiCad or Alkaline batteries. It supports a single inductor, 4-switch, buck-boost topology, which is ideal for an output voltage that is within the input voltage range. The high level of integration yields a simple, low parts-count solution. The LTC3785 provides for current-limit and shutdown in all modes of operation (which is not normally available with boost converters).

Very high efficiency is achieved by synchronous rectification, high side drive (allowing the use of N-channel MOSFETs), $R_{DS(ON)}$ current sensing, and Burst Mode® operation for efficient light load operation. Protection features include soft-start, overvoltage, undervoltage and foldback current-limit with burp-mode or latch-off for extended faults.

3.3V, 3A Converter Operates from 2.7V – 10V Source

The circuit shown in Figure 1 utilizes the LTC3785 controller to produce a synchronous, 4-switch, buck-boost design. It provides a fixed 3.3V, 3A output from a 2.7V – 10V input. It is short-circuit protected: the controller offers a choice of recycling or latch-off protection for severe overload faults.

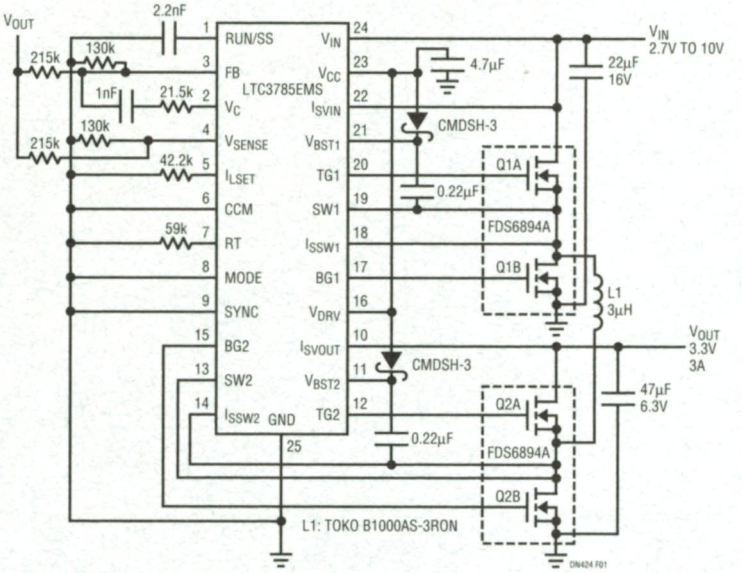

Figure 1. Schematic of Buck-Boost Converter Using the LTC3785 to Provide 3.3V at 3A from a 2.7V to 10V Source

The circuit produces seamless operation throughout the entire input voltage range, operating as a synchronous buck converter, synchronous boost converter, or a combination of the two through the transition region. At input voltages well above the output, the converter operates in buck mode. Switches Q1A and Q1B commutate the input voltage, and Q2A stays on, connecting L1 to the output. As the input voltage is reduced and approaches the regulated output voltage, the converter approaches maximum duty cycle on the input (buck) side of the bridge, and the output (boost) side of the bridge starts to switch, thus entering the buck-boost or 4-switch region of operation. As the input is reduced further, the converter enters the boost region at the minimum boost duty cycle. Switch Q1A stays on, connecting the inductor to the input while switches Q2A and Q2B commutate the output side of the inductor between the output capacitor and ground. In boost mode, this converter has the ability to limit input current, and also to shut down and disconnect the source from the output—two desirable features that a conventional boost converter cannot provide. Figures 2, 3 and 4 show input side and output side switch waveforms along with inductor current for buck (10V input), boost (2.7V input) and buck-boost (3.8V input) modes of operation.

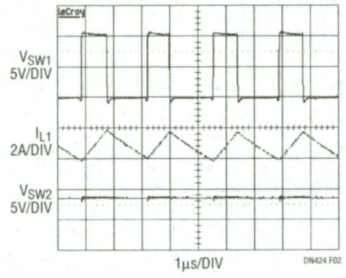

Figure 2. Input Side and Output Side Switch Waveforms Along with Inductor Current for Buck (10V Input) Mode Operation for the Circuit in Figure 1

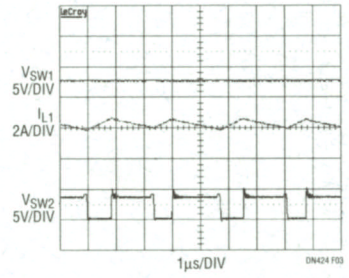

Figure 3. Input Side and Output Side Switch Waveforms Along with Inductor Current for Boost (2.7V Input) Mode Operation for the Circuit in Figure 1

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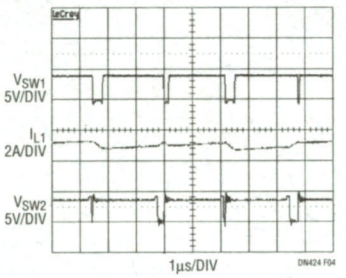

Figure 4. Input Side and Output Side Switch Waveforms Along with Inductor Current for Buck-Boost (3.8V Input) Mode Operation for the Circuit of Figure 1

95% Efficiency

Figure 5 shows efficiency curves for both normal (not forced continuous conduction) and Burst Mode operation. Exceptional efficiency of 95% is achieved at typical loads, resulting from sophisticated controller features including high side drivers and $R_{DS(ON)}$ current sensing. Even higher efficiencies are possible by using a larger ferrite inductor. This circuit easily fits in 0.6in^2 with components on both sides of the board. The curves show how Burst Mode operation improves efficiency at extremely light loads—an important determinant of battery run time.

Conclusion

The LTC3785 is the latest addition to our class of buck-boost converters developed by Linear Technology to satisfy the requirements of battery-powered applications, specifically those requiring an output voltage that is within the input voltage range. A topology based on the LTC3785 controller overcomes the deficiencies of conventional designs. It is elegant in its simplicity, high in efficiency, and requires only a small number of inexpensive external components.

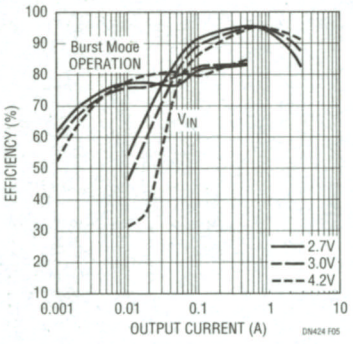

Figure 5. Efficiency in Normal and Burst Mode Operation for the Circuit in Figure 1

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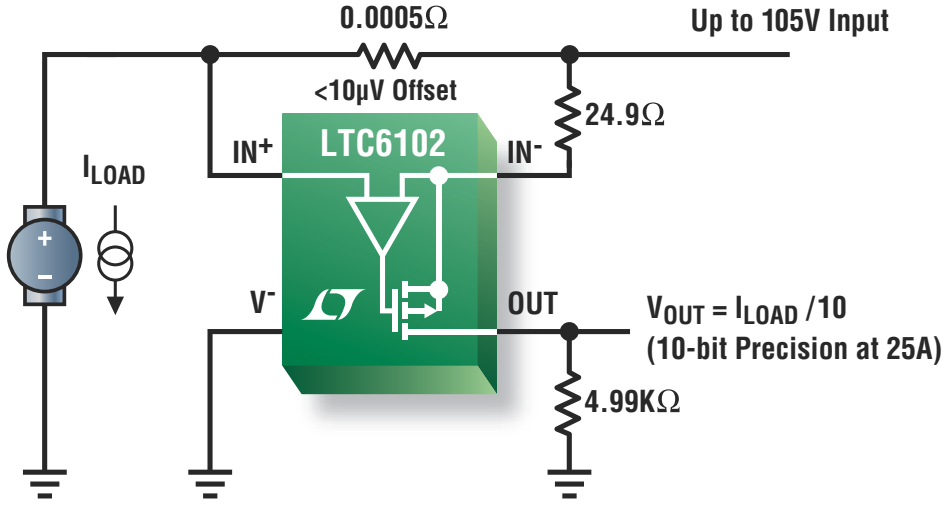

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	NEW	NEW	NEW	NEW	NEW			
Part	**LT®6106**	**LT6105**	**LTC6104**	**LTC6103 Dual**	**LTC6102 LTC6102HV**	**LTC6101 LTC6101HV**	**LT6100**	**LT1787 LT1787HV**
Current Direction	→	→	↔	→	→	→	→	↔
Common Mode Voltage	2.7V to 44V	-0.3V to 44V	4V to 70V	4V to 70V	4V to 70V 5V to 105V	4V to 70V 5V to 105V	4.1V to 48V	2.5V to 40V 2.5V to 65V
Response Time	3.5µsec	3.5µsec	1µsec	1µsec	1µsec	1µsec	40µsec	10µsec
V_{OS} Max.	250µV	300µV	450µV	450µV	10µV	300µV	300µV	100µV
V_{OS} Drift	1µV/°C	1µV/°C	1.5µV/°C	1.5µV/°C	50nV/°C	1µV/°C	0.5V/°C	0.5V/°C
I_{BIAS} Max.	40nA	25µA	170nA	170nA	3nA	170nA	10µA	20µA
Gain	R-SET	R-SET	R-SET	R-SET	R-SET	R-SET	PIN-SET	8V/V
PSRR Min.	106dB	100dB	110dB	110dB	120dB	118dB	105dB	120dB

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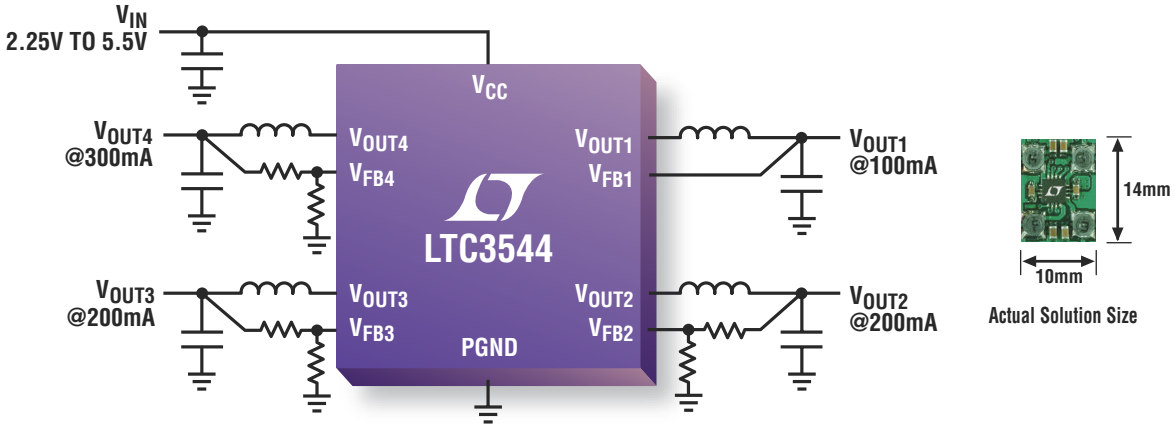

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Selected Multi-Output Synchronous Buck Converters

Part No.	Configuration	V_{IN} Range	Output Current (A)	V_{OUT} Min. (V)	Switching Frequency	Quiescent Current I_Q(µA)*	Package
LTC3547/B	Dual Synch Step-Downs	2.5V to 5.5V	0.3 x 2	0.6	2.25MHz	40	2mm x 3mm DFN-8
LTC3407/A	Dual Synch Step-Downs	2.5V to 5.5V	0.6 x 2	0.6	1.5MHz	40	3mm x 3mm DFN-10, MSOP-10E
LTC3419	Dual Synch Step-Downs	2.5V to 5.5V	0.6 x 2	0.6	2.25MHz	35	3mm x 3mm DFN-8, MSOP-10
LTC3548/-1/-2	Dual Synch Step-Downs	2.5V to 5.5V	0.8, 0.4	0.6	2.25MHz	40	3mm x 3mm DFN-10, MSOP-10E
LTC3407-2/-3	Dual Synch Step-Downs	2.5V to 5.5V	0.8 x 2	0.6	2.25MHz	40	3mm x 3mm DFN-10, MSOP-10E
LTC3417A	Dual Synch Step-Downs	2.25V to 5.5V	1.5, 1	0.8	2.25MHz	125	3mm x 5mm DFN-20, TSSOP-20E
LTC3446	Single Synch Step-Down + Dual VLDOs	2.7 to 5.5V	1.0, 0.3, 0.3	0.4	2.25MHz	140	3mm x 4mm DFN-14
LTC3545	Triple Synch Step-Downs	2.25V to 5.5V	0.6 x 3	0.6	2.25MHz	58	3mm x 3mm QFN-16, MSOP-10E
LTC3544/B	Quad Synch Step-Downs	2.25V to 5.5V	0.3, 2 x 0.2, 0.1	0.8	2.25MHz	70	3mm x 3mm QFN-16
LTC3562	I^2C Quad Synch Step-Downs	2.7V to 5.5V	2 x 0.6, 2 x 0.4	0.6	2.25MHz	100	3mm x 3mm QFN-20

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CPLD's internal oscillator performs autocalibration

Rafael Camarota, Altera Corp, San Jose, CA

The MAX II CPLD family from Altera (www.altera.com) features an internal oscillator that dissipates much lower power than do external oscillators. The internal oscillator has an accuracy of only ±25%, sometimes limiting its usage. For example, many applications, such as an interval timer for data gathering and a real-time clock, require more accuracy—±0.1 and ±0.001%, respectively. A simple circuit uses an external crystal oscillator to calibrate a timer to better than ±0.3% accuracy. The internal oscillator sustains the calibrated output even after you shut down the external oscillator to save power. The circuit maintains this accuracy as long as the V_{CC} and temperature are stable. Whenever you enable the external oscillator, the circuit quickly recalibrates if necessary.

A remote industrial sensor should sample an event every second. To save power, a timer powers down most of the sensor circuit most of the time to increase battery life. The system powers up for a short sample; then, the system, except for the CPLD, powers down, which times the period to the next power-up, sample, and calibration. Most of the components of a wireless receiver in a power-saving mode power down; however, the CPLD timer and wake-up mode stay on for monitoring and calibration.

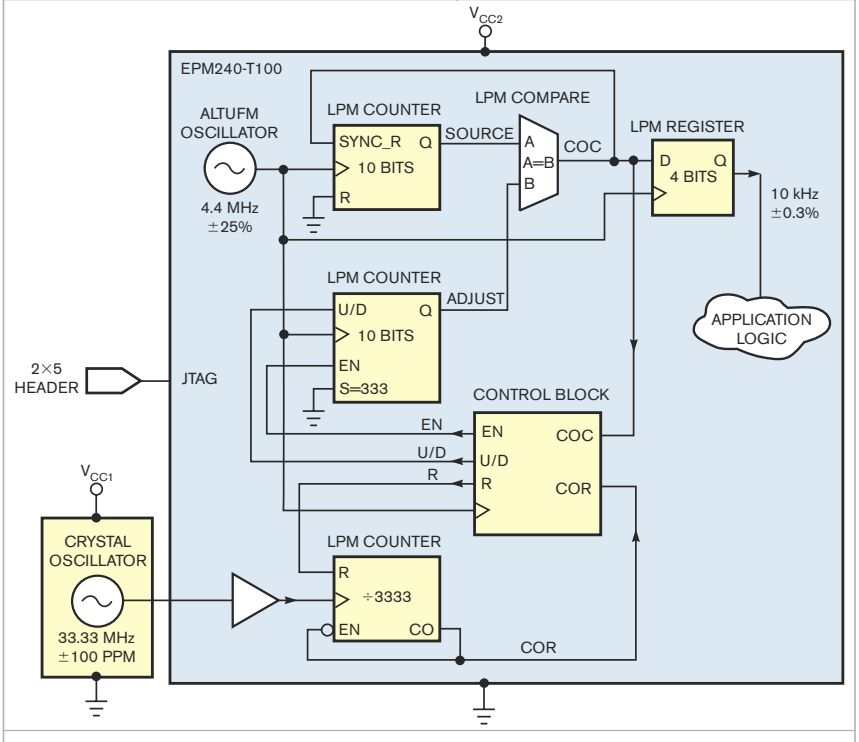

Figure 1 This internal CPLD counter first synchronizes with an external clock to ±0.3% accuracy and stays at that frequency until reset.

Figure 1 shows a simple circuit with a crystal oscillator with typical ±100-ppm accuracy; an EPM240 CPLD with a ±25%-accurate, 4.4-MHz internal oscillator; and an autocalibration circuit in the programmable-logic array that generates a ±0.3%-accurate, 10-kHz clock. For simplicity, the **figure** omits the external oscillator's V_{CC1} power-down or enable circuit and the application logic using the 10-kHz clock. The 33.33-MHz clock drives a reference counter, which is a divide-by-3333 LPM (library-of-parameterized-macros) counter. You derive LPM blocks from Altera's Quartus II LPM. The COR (carry-out-reference) signal feeds back to the count-enable input such that the COR signal stays at one after reaching the 3333 count until you apply the reset signal. The divide-by-3333 counter generates a 0.1-msec reference period. The 4.4-MHz LPM oscillator drives all other clocks in the autocalibration circuit: the source

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counter, a 10-bit counter with a power-up asynchronous reset; a synchronous reset; and a 10-bit output source. The 4.4-MHz clock also drives the 10-bit up/down-adjust counter that presets to 333 at power-up. It has an enable input, an up/down-control-input signal, and a 10-bit output adjustment. The adjust and source drive the inputs of the compare LPM that generates a one on the COC (carry-out-from-comparator) signal when adjust equals the source. The COC signal drives the synchronous input of the source counter, making it a free-running counter with a period equal to the adjustment signal. An LPM register converts the COC signal into a synchronous, 10-kHz pulse when you calibrate the system. The control-logic block generates enable, up/down, and synchronous-reset output signals based on the COC and COR inputs.

Figure 2 shows the operation of the control-block state machine. It also illustrates how the 10-kHz signal calibrates to the oscillator input. The system powers up in the start state, and the source and reference counters both start counting. Adjust starts at 333, the minimum count that the slowest variation of the LPM oscillator would require to generate a 10-kHz clock. The COR signal typically goes high before the COC signal. This action moves the state machine to the slow state, enabling the adjust counter in the up mode. It counts up from 333 until the source equals the reference, removing most of the difference between adjust and the value necessary to achieve calibration. Once the source equals the reference, the state machine moves to the calibrate state. Calibrate disables the adjust counter and resets the reference counter. The free-running source counter resets at the same time.

The COR signal will likely occur again before the COC signal and will repeat the last sequence. Eventually, the COC signal will happen before the COR signal, moving the state machine to the sustain state. In this state, the adjust counter is disabled. Once the COR signal goes high, the COC signal comes around again, making the COC and COR signals ones. The state machine then goes to the fast state. Fast enables the adjust counter in the down mode, resets the reference counter, and then goes to start. The free-running source counter resets at the same time.

When you calibrate the circuit, the COR and COC signals occur at the same time, and the state machine goes to the calibrate state. The adjust counter remains constant, the source counter resets, and the state machine moves to start. Meanwhile, the free-running source counter resets. The system stays in this calibrated loop with an occasional cycle through slow or fast to make minor adjustments to the adjust counter. If the external oscillator stops, the COR signal stays low, resulting in the state machine's staying in the sustain state until the external clock starts again. In the sustain state, the 10-kHz output stays constant assuming no significant change in system temperature or V_{CC}.

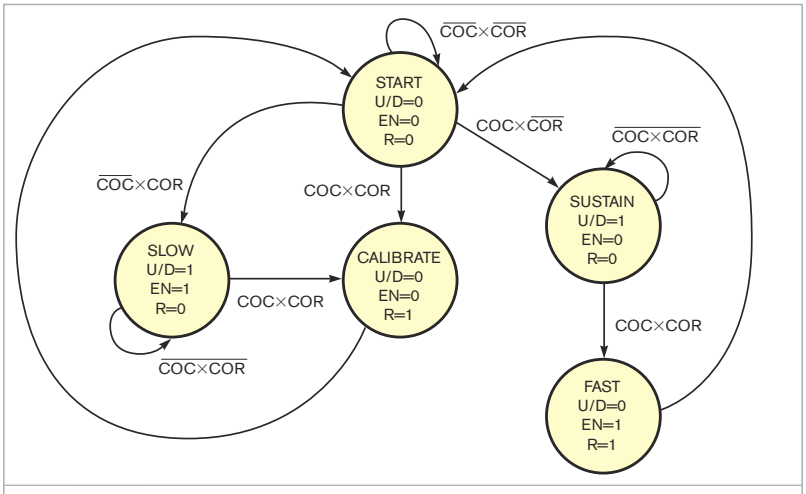

Figure 2 This state machine shows the transitions of the control block in Figure 1.

The following **equations** set the reference-count, adjust, and source-counter bit width; the adjust-counter start value; and the output-frequency accuracy: Adjust and source bit width=log2(5,555,555/output frequency) rounded up; adjust-start value=3,333,333/output frequency; reference-counter period=external-oscillator frequency/output frequency; output-frequency error=±1%/(3,333,333/output frequency); maximum output jitter=±1/3,333,333 sec; and maximum calibration time=output frequency×5.

You can achieve accuracy better than ±0.3% with a slower output frequency, but it cannot exceed the accuracy of the external oscillator. Therefore, you can build a real-time clock with a 0.01-second resolution and ±0.003% accuracy. EDN

Swapping bits improves performance of FPGA-PWM counter

Stefaan Vanheesbeke, Ledegem, Belgium

When you need some analog outputs and you have an FPGA in your system, you probably choose to use a PWM module and a simple low-pass filter such as those in **Figure 1**. The output of the FPGA is typically a waveform with a fixed-frequency, variable-duty cycle, which a counter and a digital comparator generate (**Listing 1**).

Suppose that Enable is high, the counter counts up every clock cycle,

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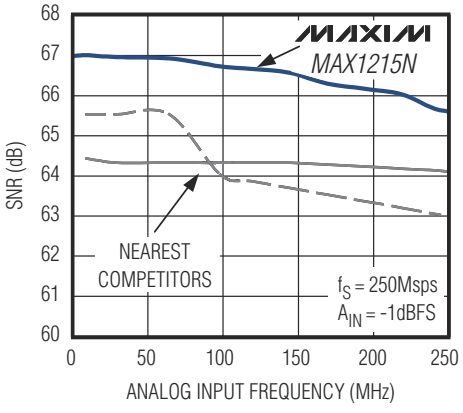
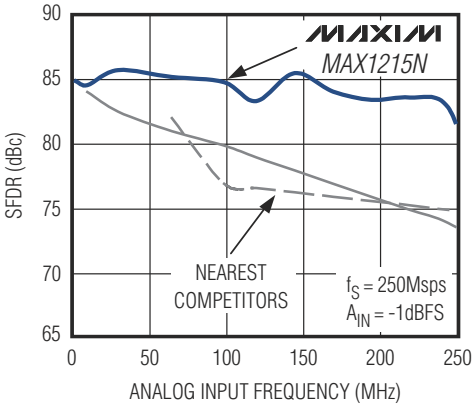


BEST SFDR AT ANY INPUT FREQUENCY



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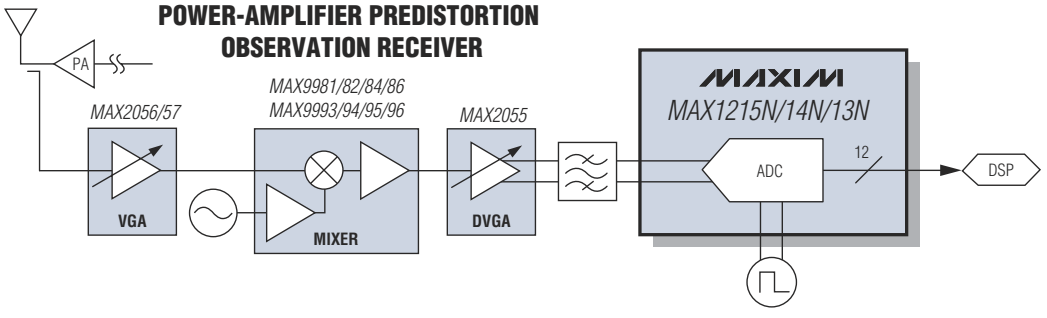

	Part	Resolution (Bits)	Speed (Msps)	No. of Channels	SNR (dB) f_{IN} = 100MHz, -1dBFS	SFDR (dBc) f_{IN} = 100MHz, -1dBFS	Integrated Buffer	Power (mW)	Interface
NEW	MAX1215N	12	250	1	66.7	85		886	LVDS
NEW	MAX1214N	12	210	1	67	81		799	LVDS
NEW	MAX1213N	12	170	1	67.2	87		720	LVDS
	MAX1215/14/13	12	250/210/170	1	65.5/65.6/65.5	70.7/74/68	✔	1006/820/788	LVDS
	MAX1219/18/17	12	210/170/125	2	66.6/67.1/67	81/82/85		1600/1400/1300	LVDS
	MAX19542/41	12	170/125	1	64.3/65	73/77	✔	907/861	CMOS
	MAX1124/23/22	10	250/210/170	1	56.8/57.4/57.1	71/74.5/72	✔	477/460/460	LVDS
	MAX1121	8	250	1	48.8	68	✔	477	LVDS

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LISTING 1 FPGA OUTPUT

```
module pwm(Clk, Reset, Enable, Value, Out);

parameter CountBits = 8;

input  Clk, Reset;
input  Enable;
output Out;
input  [CountBits-1:0] Value;

reg    [CountBits-1:0] Count;

assign Out = Count < Value;

always @(posedge Clk or posedge Reset)
  if (Reset)
    Count <= 0;
  else
    if (Enable)
      Count <= Count + 1;

endmodule
```

LISTING 2 REWIRING MODIFICATION

```
module pwm(Clk, Reset, Enable, Value, Out);

parameter CountBits = 8;

input  Clk, Reset;
input  Enable;
output Out;
input  [CountBits-1:0] Value;

reg    [CountBits-1:0] Count;

reg [CountBits-1:0] Swapped;
integer k;
always @*
  for (k = 0; k < CountBits; k=k+1)
    Swapped[k] = Count[CountBits-1-k];

assign Out = Swapped < Value;

always @(posedge Clk or posedge Reset)
  if (Reset)
    Count <= 0;
  else
    if (Enable)
      Count <= Count + 1;

endmodule
```

and the frequency of the PWM output is the clock frequency divided by 2 count bits. You can use Enable to lower the output frequency by connecting it to a prescaler. Because the output frequency is fixed, the filter is easy to calculate, because you know that the worst-case ripple happens at a duty cycle of 50%. The combination of the desired maximum ripple and settling time determines the filter type and RC (resistance/capacitance) values.

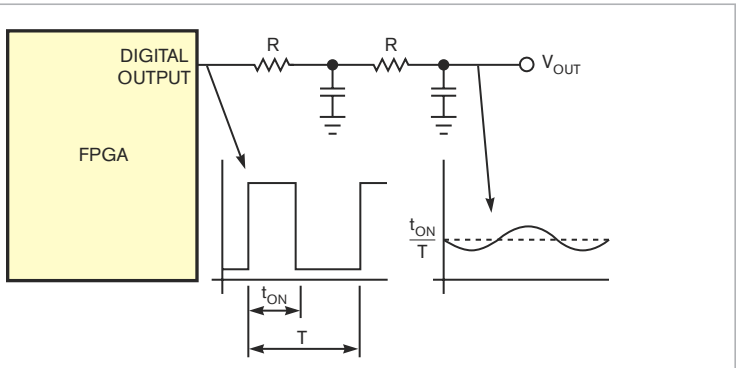

Figure 1 A simple lowpass filter changes the PWM digital output from an FPGA to an analog voltage level. The maximum ripple occurs at a 50% duty cycle.

LISTING 3 SIMULATION RESULTS

```
Simulation results :

Testing   0 : 0000000000000000
Testing   1 : 0000000000000001
Testing   2 : 0000000100000001
Testing   3 : 0001000100000001
Testing   4 : 0001000100010001
Testing   5 : 0101000100010001
Testing   6 : 0101000101010001
Testing   7 : 0101010101010001
Testing   8 : 0101010101010101
Testing   9 : 1101010101010101
Testing  10 : 1101010111010101
Testing  11 : 1101110111010101
Testing  12 : 1101110111011101
Testing  13 : 1111110111011101
Testing  14 : 1111110111111101
Testing  15 : 1111111111111101
```

With a small change to the code in **Listing 1**, you can improve the performance of the PWM circuit. Whereas in the original system, the maximum ripple currents occur at a duty cycle of 50% and the minimum ripple currents occur at the minimum duty cycle, the improved version shows a maximum ripple equal to the minimum of the standard version. The trick is to generate the highest frequency possible but keep the average duty cycle constant. The higher the frequency of the pulses on the output, the better the filter does its job.

The modification to **Listing 1** consists of rewiring the binary comparator with all the bits swapped from left to right. The MSB (most significant bit) becomes the LSB (least significant bit), the LSB becomes the MSB, and so on (**Listing 2**). You do only a rewiring requiring no extra registers or logic.

Listing 3 shows the pulse trains that a 4-bit PWM emits. In **Listing 3**, you see that at 50% duty cycle (Value=8, second column), the frequency is maximum and equal to the clock frequency divided by two. At the first point at which some ripple shows up (Value=1, second column), there is exactly the same ripple as in the conventional PWM system—that is, the pulse train is the same. EDN

Relays eliminate high-voltage noise

Jui-I Tsai, Woei-Wu Pai, Feng-Chang Hsu,
Po-Jui Chen, Ching-Cheng Teng, and Tai-Shan Liao,
National Applied Research Laboratories, Hsinchu, Taiwan

Most laboratories and industrial environments have many kinds of electrical-noise sources at all frequencies from heavy machinery, instruments, power supplies, and TV stations. Engineers have used many simple devices and techniques to handle this noise. These techniques include the use of proper grounding methods, shielded and twisted wires, signal averaging, differential-input-voltage amplifiers, and filters. Although these methods can control and reduce the noise in most measurements, some techniques just prevent noise from entering the system, whereas others remove only extraneous noise from the signal. These methods usually find use only in low-voltage sys-

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DS2432**	1kb EEPROM with SHA-1	1-Wire®	Bidirectional SHA-1 challenge and response
DS28E01-100**	1kb EEPROM with SHA-1	1-Wire	Bidirectional SHA-1 challenge and response
DS2401/DS2411	64-bit ROM serial number	1-Wire	Customized 64-bit ROM
DS28CM00	64-bit ROM serial number	I²C/SMBus	Customized 64-bit ROM
DS2431	1kb EEPROM	1-Wire	Customized 64-bit ROM, WP/OTP modes
DS2460**	SHA-1 coprocessor	I²C	Secure storage of system secrets

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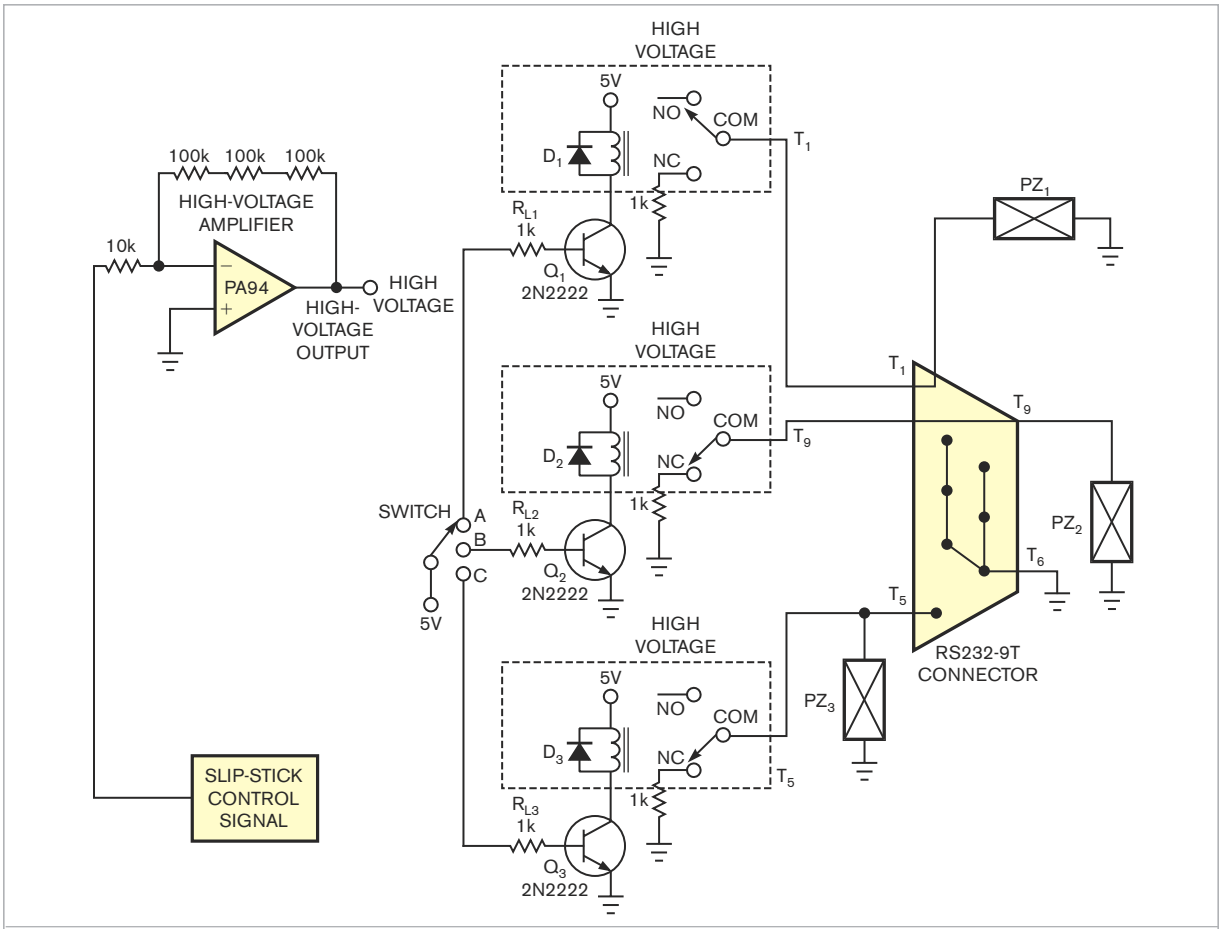

Figure 1 This simple circuit connects unenergized inputs to ground through a resistor.

tems; they do not address high-voltage-induced noise. This Design Idea offers a practical approach to reducing high-voltage-induced noise. The floating input of a scanning electron microscope has high impedance, and it acts as an antenna, picking up noise signals. The microscope's actuators need a high-voltage signal to drive their piezoelectric slip-stick stack motors. The motion mechanism requires a ramping waveform spanning to 800V p-p. The mechanism requires multiple channels because there are three degrees of tip motion. Some microscopes incorporate optical-path-adjustment microsliders for atomic-force microscopy; those scopes need even more channels.

Traditionally, each channel needs a high-voltage amplifier. So, two degrees of tip motion need two high-voltage amplifiers, three degrees need three amplifiers, and so on. High-voltage amplifiers are expensive and need considerable space on the PCB (printed-circuit board), however. Therefore, controlling multiple degrees of tip motion using only one high-voltage amplifier that switches among multiple channels saves cost and space. The pins of high-voltage connectors have enough space between them to avoid disturbing adjacent signals. But high-voltage connecters are expensive and too large to easily arrange. So, the best choice is to use a commercial RS-232-standard, nine-pin/25-pin connector (**Figure 1**). The pins of most commercial RS-232 connectors are close enough together to easily pick up induced high-voltage signals. You can solve this problem by connecting a low impedance to the floating pins of the RS-232 connector.

THE FLOATING INPUT OF A SCANNING ELECTRON MICROSCOPE HAS HIGH IMPEDANCE, AND IT ACTS AS AN ANTENNA, PICKING UP NOISE SIGNALS.

In this circuit, three piezoelectric motors, PZ_1, PZ_2, and PZ_3, connect to the T_1, T_5, and T_9 pins of the RS-232-9T connector. The circuit has three relays that switch the high-voltage input to the piezoelectric motors. The normally open node of the relays connects to the high-voltage-amplifier output. The normally closed nodes of the relays connect to three 1-kΩ resistors to bypass high-voltage-induced noise to ground. EDN

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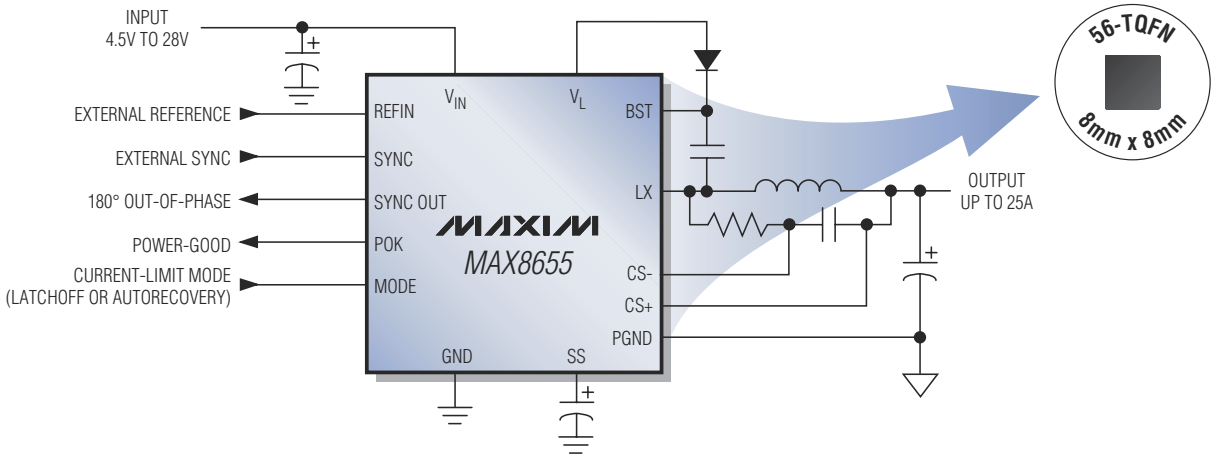

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VHDL program enables PCI-bus-arbiter core

Antonio Di Rocco, Selex Communications, Chieti, Italy

This Design Idea describes a VHDL implementation of a PCI 2.2-bus arbiter (**Figure 1**). Any PCI system may have one or more PCI-master devices. Most devices can behave as target hosts, but one must be a PCI-bus initiator, or master. Normally, only microprocessors or high-level DSPs perform both PCI master and target modes, and they may include a PCI arbiter. **Listing 1**, a simple VHDL program, is available at www.edn.com/070913di. It performs an arbitration function by enabling access to the PCI bus depending on the predetermined priorities of each PCI device. The PCI-arbiter core interfaces with 33- and 66-MHz PCI systems, supports as many as six PCI-bus masters, supports "bus parking," enables a pure rotational-arbitration scheme, supports bus latency and broken masters, and is a synthesizable VHDL source without FGPA- or PLD-library intellectual property.

The PCI bus supports more than one master device. If only one master requests the bus, that master immediately gets the grant. If several devices simultaneously require the use of the PCI bus to perform a data transfer, they assert their request signal, REQ_N, to the arbiter. The one with highest priority gets the GNT_N grant. After that, the one with the second highest priority has the highest priority, and so on. The PCI_RST assertion resets the arbiter's priority-shift register to device 0.

The PCI bus has no pullups on the AD bus and C/BE lines. To avoid having these signals float for a long period, PCI designs must implement bus parking, meaning that a master device drives the AD bus and C/BE lines during bus-idle states. The arbiter selects which master will be park master. The arbiter asserts GNT_N of the park master, even though the park master did not assert REQ_N. The constant "Bus_parker" in the VHDL code defines the park master. After a device has access to the PCI bus, this device must start the bus access within 16 PCI clock cycles. If this start-up does not happen, the device loses the bus grant, and the device with the next highest priority gets the bus. To check bus latency, the arbiter must check the signals FRAME_N and IRDY_N. The PCI-arbiter core fits into any PLD or FPGA and consumes few resources. EDN

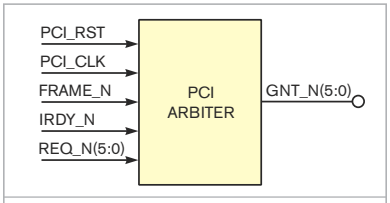
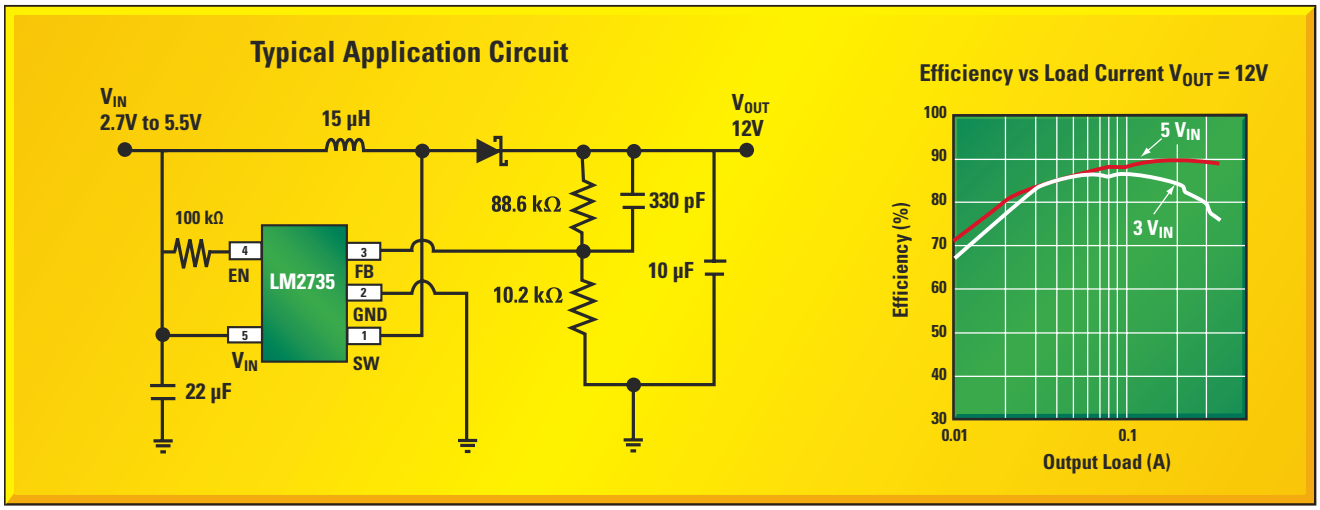


Figure 1 This PLD/FPGA-based PCI-bus arbiter grants bus requests based on a simple rotational-priority scheme.

Tiny Boost Regulator Provides Ease-of-Use and High Output Current

LM2735 Delivers 2.1A Switch, Internal Compensation in Tiny Packages



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Easy-to-Use, Small Solution Size

- Internal compensation allows for ease-of-use and minimal external components
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SOT-23 Boost Regulators

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Product ID	V_{IN} Range	Switch Current	V_{OUT} Max	Frequency	Ideal For	Package
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LM2733	2.7V to 14V	1A	40V	600 KHz 1.60 MHz	TV tuners, set top boxes, white LED current sources	SOT23-5
NEW LM2735	2.7V to 5.5V	2.1A	24V	520 KHz 1.60 MHz	LCD and OLED displays for portable applications, USB powered devices, white LED current source	SOT23-5 LLP-6, eMSOP-8

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LINKING DESIGN AND RESOURCES

Start-up customers: diamonds in the rough

A diamond in the rough may be a hard find, but Avnet Electronics Marketing (Avnet EM, www.em.avnet.com) believes it is worth the search. Avnet EM recently set out on such a search and came across Black Diamond Advanced Technology (www.bdatech.com) and its SwitchBack Ultra Mobile PC.

The SwitchBack targets the commercial and industrial segment, and Black Diamond designed and built it to withstand intense shock, moisture, vibration, dust, and extreme temperatures. Weighing three pounds and measuring 7.5×5.5×2 in., the SwitchBack allows users to add devices to it with its customized BackPack Module.

With such a unique product and being a small start-up, says Justin Dyster, president and co-founder of Black Diamond, it was initially hard for the company to find backing and support. "When companies came by to see us, there was a lot of skepticism. Avnet saw the vision of what we were doing early on and helped us overcome some of those hurdles."

Steve Markey, an Avnet account manager with the distributor for more than 20 years, first found Black Diamond. Armed with his electronics-supply-chain expertise and contacts, he began working with Black Diamond from day one.

"Black Diamond was as small as you can get," says Joe Tillison, technical marketing director at Avnet EM. "[Our] account manager … was able to use his relationship and contacts in the industry to bring in the right reps and the right suppliers to get what [Black Diamond] needed."

Tillison cites Avnet EM's link to Toshiba (www.toshiba.com), the supplier of the SwitchBack's sunlight-readable display, and the distributor's introduction of Black Diamond to Intel (www.intel.com), which led to the use of its technology in an Intel-commissioned motorcycle for an episode of *American Chopper*.

Tillison notes that work with start-ups doesn't always turn out to be successful. But some do. "And when we can pick the winner and work closely with [it], it's a benefit to us. We grow with [it]."

Black Diamond expects volume to surpass 3000 units a year and estimates the SwitchBack's starting price at $5000.

GREEN UPDATE

NORWAY POHS CASTS WIDE NET

Norway is casting a wide net with its latest environmental directive, a set of ROHS (restriction-of-hazardous-substances)-like rules that aim to restrict or ban 18 substances used in consumer goods.

Norway's POHS (prohibition on certain hazardous substances) in consumer products is similar to the EU's (European Union's) ROHS directive. Yet, it is vastly different. Of the 18 substances POHS looks to restrict or ban, only lead and cadmium are common to EU ROHS, which restricts or bans six substances. EU ROHS also applies directly to electrical and electronic equipment; POHS targets consumer equipment, which it defines as "any product that is intended for consumers or that can reasonably be expected to be used by consumers." Of specific threat to the electronics supply chain is the possible blacklisting of GaAs (gallium arsenide) through the proposal's arsenic restriction.

POHS will apply only to trade in Norway. However, unless under exemption, electronics producers selling into the country that have collected EU ROHS-compliance certificates will need to again obtain certification from suppliers certifying that components use none of the 18 POHS substances.

The Norwegian proposal aims for implementation as an additional chapter in the Norwegian Product Regulations legislation and is currently the subject of public consultation. POHS adoption is scheduled for Dec 15, 2007, and the directive is expected to come into force on Jan 1, 2008.

OUTLOOK

OUTSOURCING BY OEMs PUSHES EMS, ODM GROWTH

Current dynamics in the electronics-contract-manufacturing market point to further outsourcing by OEMs (original-equipment manufacturers), and, as a result, both EMS (electronics-manufacturing-service) providers and ODMs (original-design manufacturers) will enjoy steady growth through 2013, according to Frost & Sullivan (www.smt.frost.com).

Research from the company finds that the EMS market saw sales of $190 billion in 2006 and estimates that figure will reach $387.42 billion in 2013. Meanwhile, the research shows that the ODM market earned lower revenues of $100.65 billion in 2006 but estimates that those revenues will more than double to reach $219 billion in 2013.

Frost & Sullivan points to increased outsourcing from automotive and communication industries and new outsourcing opportunities from the likes of aerospace and defense as likely drivers of the future growth for the EMS market.

The company notes that design expertise represents a primary growth factor for ODMs, especially in markets such as consumer electronics, in which OEMs often seek ODMs as strategic design partners.

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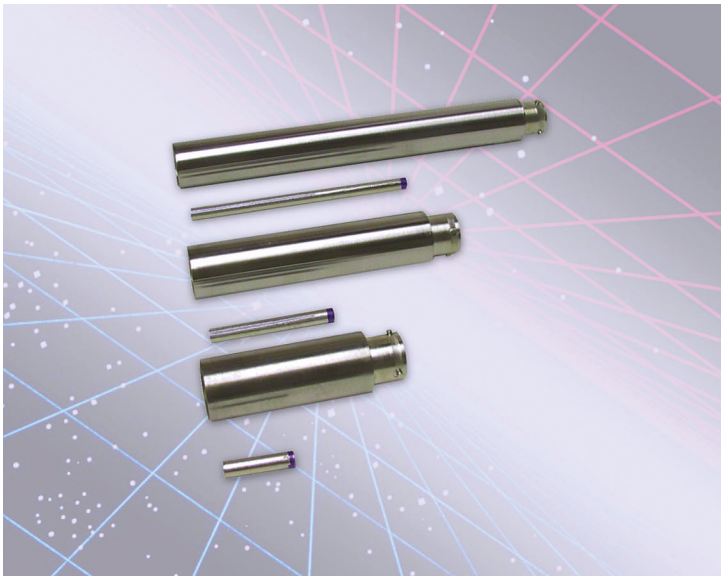
productroundup

SENSORS AND TRANSDUCERS



LVDT-position transmitters operate in hostile environments

Targeting position monitoring and feedback, the hermetically sealed HIS/R 750 loop-powered LVDT (linear-variable-displacement-transducer)-position-transmitter series functions in hostile environments and suits mechanical-position measurement in which you can make a hard connection to a test piece. The devices' 4- to 20-mA-current-loop I/O enables field integration with PLCs (programmable-logic controllers), digital indicators, host-computer-based data processing, and QC (quantum-cryptography) data-collection systems. Configurable for loop-powered, two-wire sourcing inputs or externally powered, three-wire sourcing outputs, the devices suit I/O requirements in various applications. Features include ±0.10% linearity for precision measurement and 0.25% maximum-linearity error of the full-range output using a statistically best-fit straight line derived by the least-squares method. The HIS/R position transmitters measure 2.5 to 500 mm with a 19-mm diameter and costs $591 to $900, depending on options.

Macro Sensors, www.macrosensors.com

Analog accelerometer integrates a MEMS sensor and CMOS-interface chip

An addition to the vendor's low-g linear-accelerometer line, the two-axis LIS244AL analog accelerometer combines a dual-axis MEMS (microelectromechanical-systems) sensor and a CMOS-interface chip providing two simultaneous, real-time analog outputs. The outputs feature a lateral output for the side-to-side direction and a longitudinal output for forward and backward directions. The device has a 10,000g shock survivability and provides a ±2g full-scale output range. In a 4×4×1.5-mm package, the LIS244AL costs $2.30 (10,000).

STMicroelectronics, www.st.com

RTD temperature-sensor family has a variety of resistance values

The nickel-thin-film RTD (resistance-temperature-detector) sensors provide a large change resistance in response to temperature changes. The sensors feature 100, 120, 500, and 1000Ω resistance values. Available temperature coefficients include 6180 ppm, suiting DIN 43760; 6370 ppm, suiting the HVAC curve; and 6720 ppm, suiting ANSI standards. The nickel-thin-film RTD sensor costs $2 (5000).

DWM & Associates, www.dwmai.com

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LOOKING AHEAD

TO THE 123rd US AES CONVENTION

The Javits Center in New York hosts the 123rd US AES (Audio Engineering Society) Convention for all things audio from Oct 5 through 8. Technical sessions span the range from studies in human perception of sound to the use of psychoacoustic modeling in digital-signal processing to the application of multicore processors. One session covers the problems of audio reproduction in automobiles, where lots of people listen to music. The keynote address is a mystery story: a review of the music of composer Ludwig van Beethoven, his deafness, and the slowly accumulating medical understanding that still falls short of explaining either his condition or his ability to work despite it.

LOOKING BACK

AT A MICROCONTROLLER OF THE 1950s

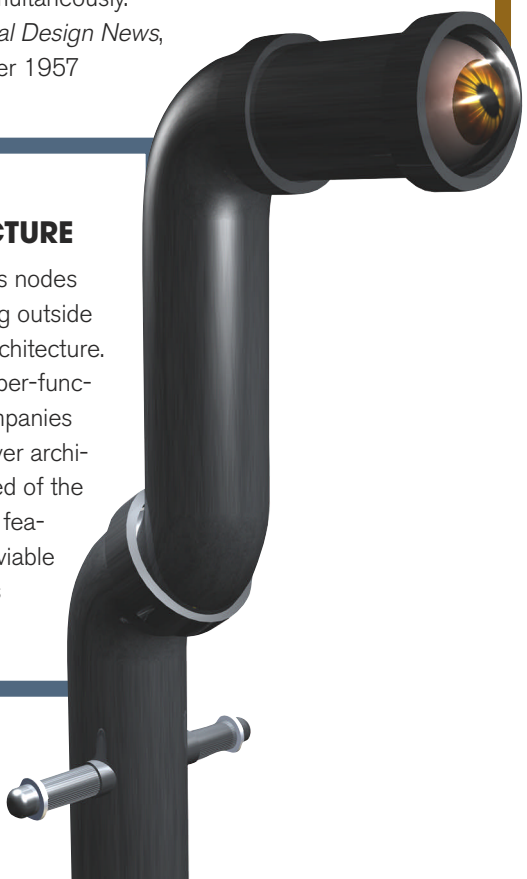
Ramo-Wooldridge Corp has designed a fully transistorized digital-control computer to provide automatic control for manufacturing processes. The 55×29×36-in. unit automatically reads process instruments, performs necessary computations to relate readings to process objectives, determines appropriate actions, and activates process mechanisms. The RW-300 computer uses a 3600-rpm magnetic-drum memory with a storage capacity of almost 8000 words, allowing storage for several programs simultaneously.

—*Electrical Design News*, September 1957

LOOKING AROUND

AT THE IMPORTANCE OF SOC ARCHITECTURE

As the cost of design and manufacturing at new process nodes continues to increase, there is increasing value in looking outside the box for a new approach to SOC (system-on-chip) architecture. Even though the cost of design is still going down on a per-function basis, most start-ups and many moderate-sized companies can no longer fund a design of any size at 65 nm. A clever architecture that reduces both the size and the required speed of the hardware can pay huge dividends by making the design feasible in a more mature process, making a chip design a viable alternative to knuckling under and using someone else's standard-product IC.



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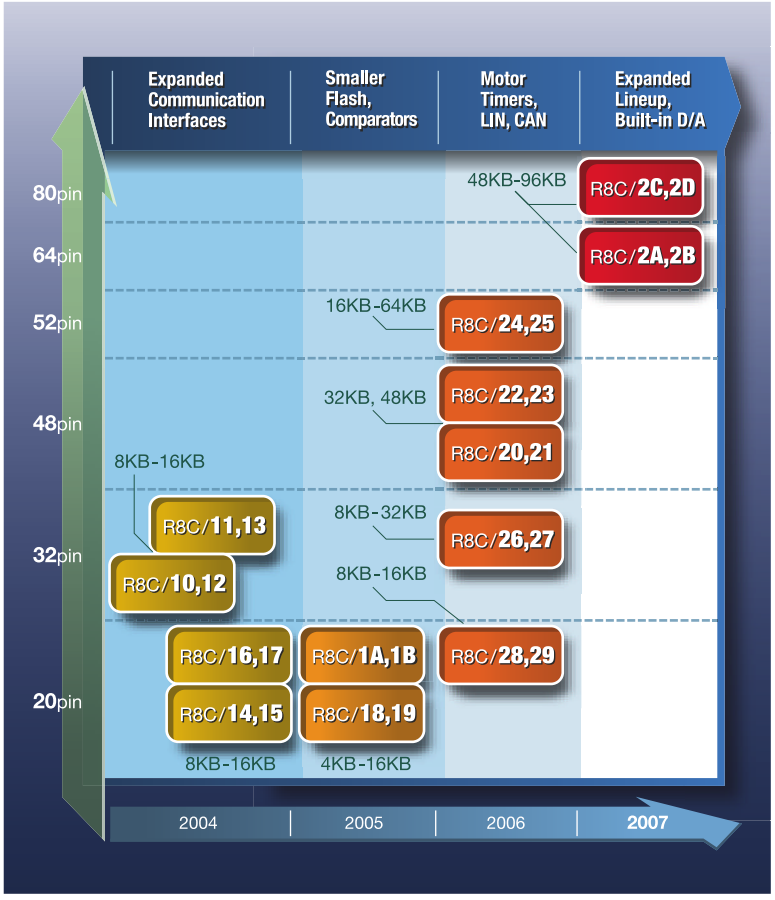
R8C/Tiny Product Roadmap



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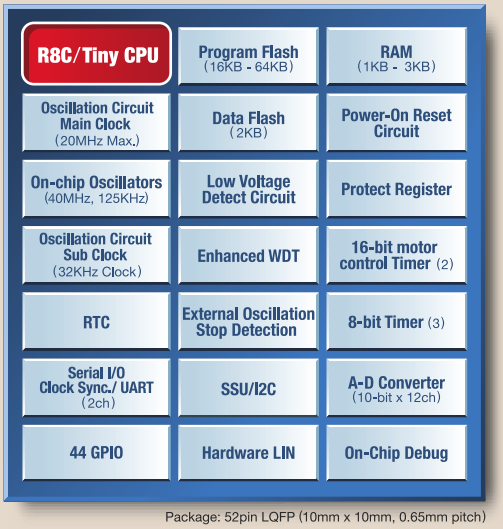

Package: 52pin LQFP (10mm x 10mm, 0.65mm pitch)

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  - 16-bit CPU runs at 20MHz, executing instructions in as fast as 50nsec.
- **Scalable**
  - Same core, same peripherals allows easy portability from 20 to 80pins
- **High-Integration**
  - Includes 40MHz on-chip oscillator, data flash, power-on reset circuits, several 8- and 16-bit timers, up to 20 channels of A/D, D/A, LIN, CAN and more
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*Source: Gartner Dataquest (April 2006) "2005 Worldwide Microcontroller Vendor Revenue" GJ06333

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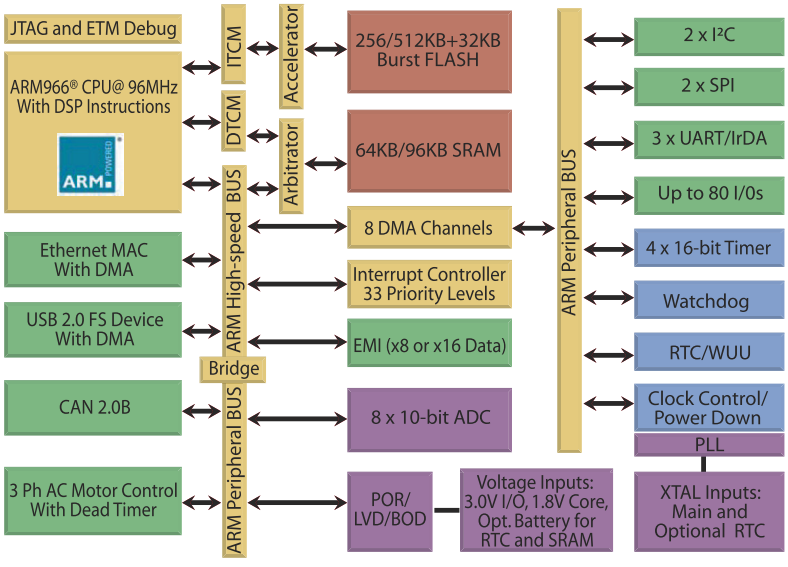

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				(IC/OC/ PWM)	Other					
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STR910FW32X	256 + 32	64	8x10-bit				80 (16)	LQFP128		CAN, EMI
STR911FM42X	256 + 32	96	8x10-bit				40 (16)	LQFP80		USB, CAN
STR911FM44X	512 + 32	96	8x10-bit				40 (16)	LQFP80		USB, CAN
STR912FW42X	256 + 32	96	8x10-bit				80 (16)	LQFP128		Ethernet, USB, CAN, EMI
STR912FW44X	512 + 32	96	8x10-bit				80 (16)	LQFP128		Ethernet, USB, CAN, EMI

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